BAT32G137 Datasheet

Ultra-low power 32-bit microcontrollers based on ARM® Cortex®-M0+

128KB Flash, analog functions, timers and communication interfaces.

V2.5.9

Features

- **Ultra-low power consumption technology**
  - Operating Voltage:2.0V~5.5V
  - Operating ambient temperature:-40℃~105℃
  - Low power modes:SLEEP, DEEPSLEEP
  - Operating power consumption:
    RUN mode: 75uA/MHz@48MHz
    DEEPSLEEP mode:0.45uA
    DEEPSLEEP mode(+32.768K+RTC):0.7uA
- **Core**
  - ARM®32-bitCortex®-M0+ CPU (MPU)
  - Operating frequency:32KHz~48MHz
- **Memories**
  - 128KB Flash Memory: program/data flash
  - 1.5KB Special data flash memory
  - 12KB SRAM Memory(With Parity)
- **Reset and power management**
  - Power-on reset circuit.
  - On-chip voltage detector (LVD) (Select interrupt and reset from 10 levels)
- **Clock**
  - High-speed on-chip oscillator, accuracy ±1%.
    Select from 1MHz to 64MHz (CPU:1MHz to 48MHz)
  - Low-speed on-chip oscillator: 15KHz
  - Main clock oscillator: 1MHz to 20MHz
  - Sub clock oscillator: 32.768KHz
- **Multiplier/divider**
  - Single-cycle integer multiplier
  - 4-cycle or 8-cycle integer divider
- **DMA**
  - Interupt trigger start.
  - Transfer modes: Normal mode, Repeat mode, Block mode and Chain transfers mode
  - Transfer space: 4 GB area from 0000 0000h to FFFF FFFFh except reserved areas
- **EVENTC**
  - Event Link Controller
  - Event signals(22 types) can be used as activation sources for operating any one of 10 types of peripheral functions
- **Analog**
  - 12-Bit A/D Converter
    Conversion range: 0 to Vrefp or VDD
    Analog input: Up to 16 channels,
    Internal reference voltage (1.45 V) and temperature sensor
    Conversionrate: 1.06Msps
  - 8-Bit D/A Converter (DAC8) × 2
  - Comparator(CMP) × 2:The external reference voltage or internal reference voltage can be selected as the reference voltage
  - Programmable gain amplifier(PGA)×2: GAIN X4/8/10/12/14/16/32Can be selected
- **GPIO**
  - I/O port:29 to 59
  - Can be set to N-ch open drain, TTL input buffer, and on-chip pull-up resistor
  - On-chip key interrupt function
  - On-chip clock output/buzzer output controller
- **Serial wire debug (SWD)**
- **Timers**
  - 16-bit timer: 9 channels
  - 15-bit interval timer: 1 channel
  - Real-time clock(RTC): 1 channel
  - Watchdog timer(WWDT): 1 channel (operable with the dedicated low-speed on-chip oscillator)
  - SysTick timer
- **Serial interfaces**
  - SPI:1 channel；Sample SPI:3 to 6 channels
  - UART:3 channels (LIN-bus)
  - I2C:1 channel；Sample I2C:3 to 6 channels
  - IrDA:1 channel
  - CAN:1 channel
- **Safety**
  - IEC/UL 60730
  - Illegal memory access
  - SRAM Parity Error Check
  - Cyclic Redundancy Check (CRC) Calculator
  - SFR protection
  - 128-bit unique ID
  - Flash secondary protection in debug mode（level1: only erase the entire area of flash; level2: the emulator connection is invalid）
- **Packages**
  - 32~48 pin

1 Overview

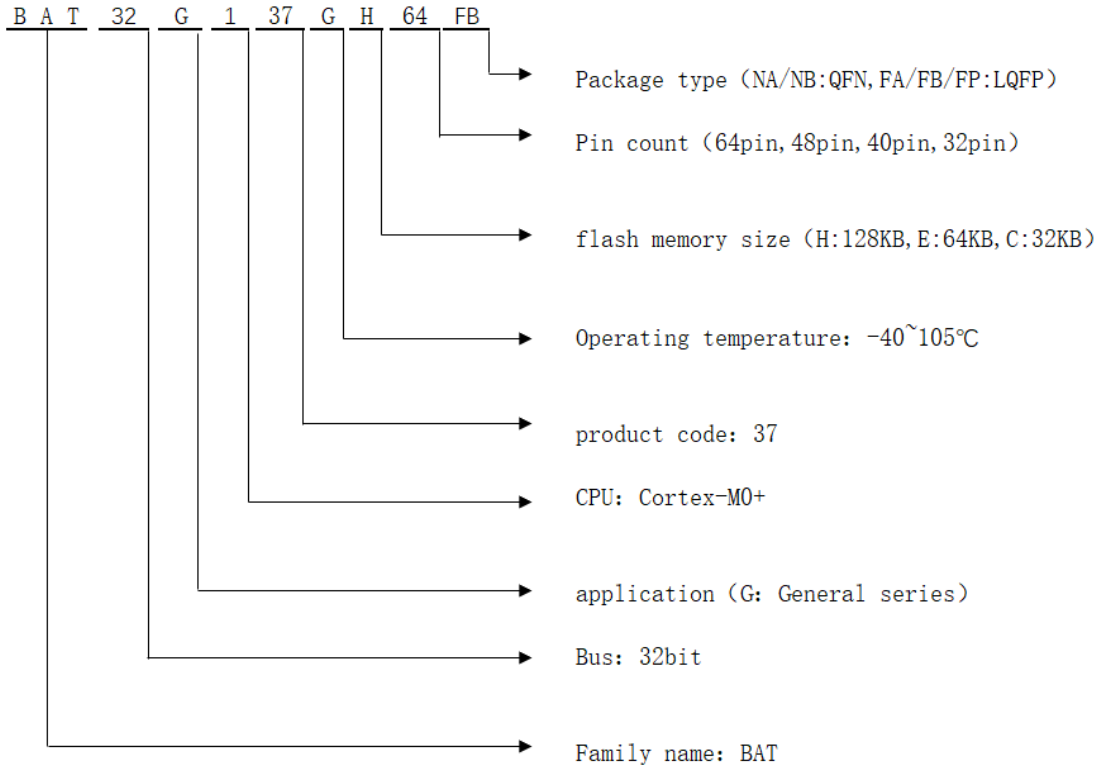
1.1 Introduction

The ultra-low-power BAT32G137 incorporates a high-performance ARM®Cortex®-M0+ 32-bit RISC core running up to 48 MHz and high-speed embedded flash memory (SRAM maximum 12KB, program/data flash 128KB). This product integrates I2C, SPI, UART, LIN multiple standard interfaces. Integrated 12bitA/D converter, temperature sensor, 8bitD/A converter, comparator, programmable gain amplifier. Among them, the 12bitA/D converter can collect external sensor signals to reduce the system design cost. The 8-bit D/A converter can be used for audio playback or power control. The temperature integrated sensor can realize real-time monitoring of the external ambient temperature. The integrated comparator can support both high-speed and low-speed operating modes. In high-speed mode, it can support feedback control of high-speed motor operation. And in low-speed mode, it can be used for battery monitoring. Integrated multiple advanced timer modules.

BAT32G137 has particularly excellent low-power performance, with two low-power modes of sleep and deep sleep, to flexible design for users. Its operating power consumption is 75uA/MHz@48MHz, and the power consumption in deep sleep mode is only 0.45uA, which is suitable for battery-powered low-power devices. At the same time, due to the integrated event link controller, direct connection between hardware modules can be achieved without CPU intervention, which is faster than the use of interrupt response, while reducing the CPU's activity frequency and extending battery life.

These features make the BAT32G137 microcontroller series widely applicable to energy storage, battery packs, motor control, security, power, and other applications.

1.2 Ordering Information



BAT32G137 Product list:

Pin count	Package	Ordering Part Number
32 pins	32LQFP (7x7mm, 0.8mm pitch)	BAT32G137GH32FP
40 pins	40QFN (5x5mm,0.4mm pitch)	BAT32G137GH40NB
48 pins	48LQFP (7x7mm, 0.5mm pitch)	BAT32G137GH48FA
64 pins	64LQFP (7x7mm, 0.4mm pitch)	BAT32G137GH64FB

FLASH, SRAM:

Flash memory	Special data flash memory	SRAM	BAT32G137	
			32 Pins	40 Pins
128KB	1.5KB	12KB	BAT32G137GH32	BAT32G137GH40

Flash memory	Special data flash memory	SRAM	BAT32G137	
			48 Pins	64 Pins
128KB	1.5KB	12KB	BAT32G137GH48	BAT32G137GH64

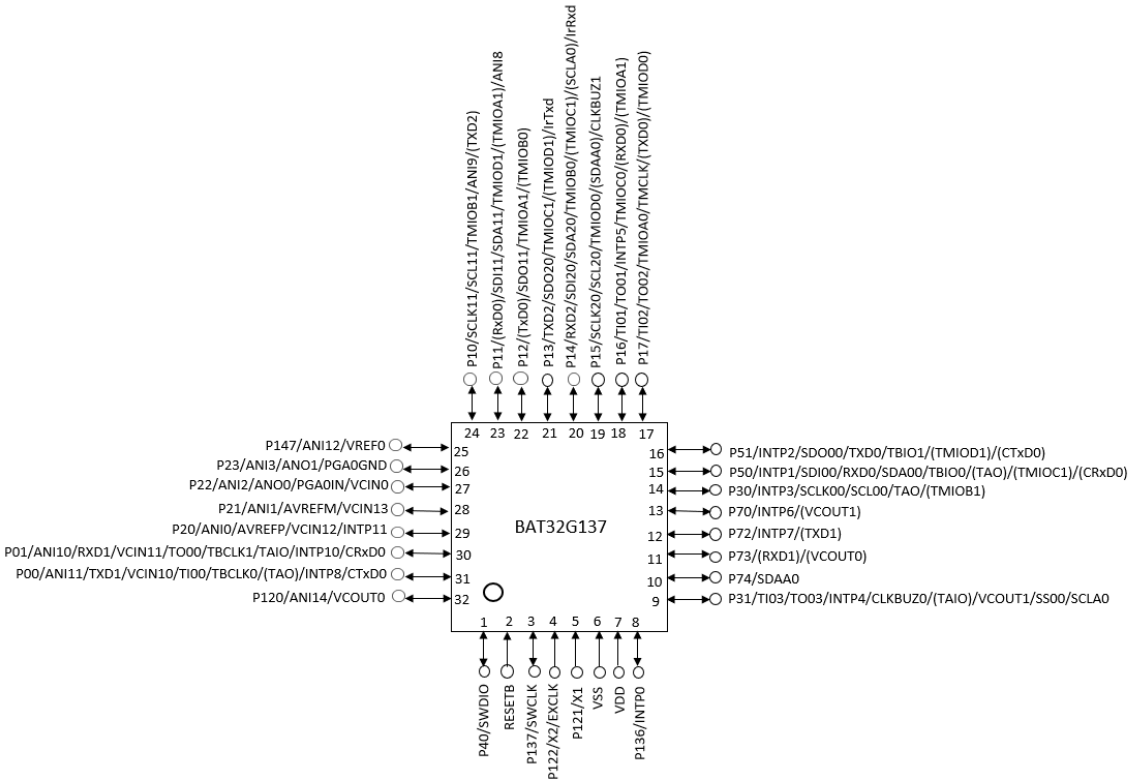
Product selection table of BAT32G137:

Part No.	kernel	Main frequency (MHz)	Minimum working voltage (V)	Maximum working voltage (V)	Code Flash (kB)	SRAM (kB)	Data Flash (kB)	DMA	GPIO	12bit ADC	8bit DAC	Comparator CMP	Amplifier PGA	Universal timer (16bit)	Real Time Clock (RTC)	Watchdog timer (WDT)	Asynchronous serial bus (UART)	Synchronous serial bus (SPI)	IIC bus	IrDA bus	LIN bus	CAN bus	Hardware multiplier	Hardware diyider	package
BAT32G137 GH32FP	M0+	48	2.0	5.5	128	12	1.5	35	29	10+3	2	2	1	9	1	1	3	3	1+3	1	1	1	Y	Y	LQFP 32
BAT32G137 GH40NB	M0+	48	2.0	5.5	128	12	1.5	36	37	12+4	2	2	2	9	1	1	3	4	1+4	1	1	1	Y	Y	QFN 40
BAT32G137 GH48FA	M0+	48	2.0	5.5	128	12	1.5	36	45	15+4	2	2	2	9	1	1	3	5	1+5	1	1	1	Y	Y	LQFP 48
BAT32G137 GH64FB	M0+	48	2.0	5.5	128	12	1.5	37	59	16+4	2	2	2	9	1	1	3	6	1+6	1	1	1	Y	Y	LQFP 64

1.3 Pin Configuration (Top View)

1.3.1 BAT32G137GH32FP

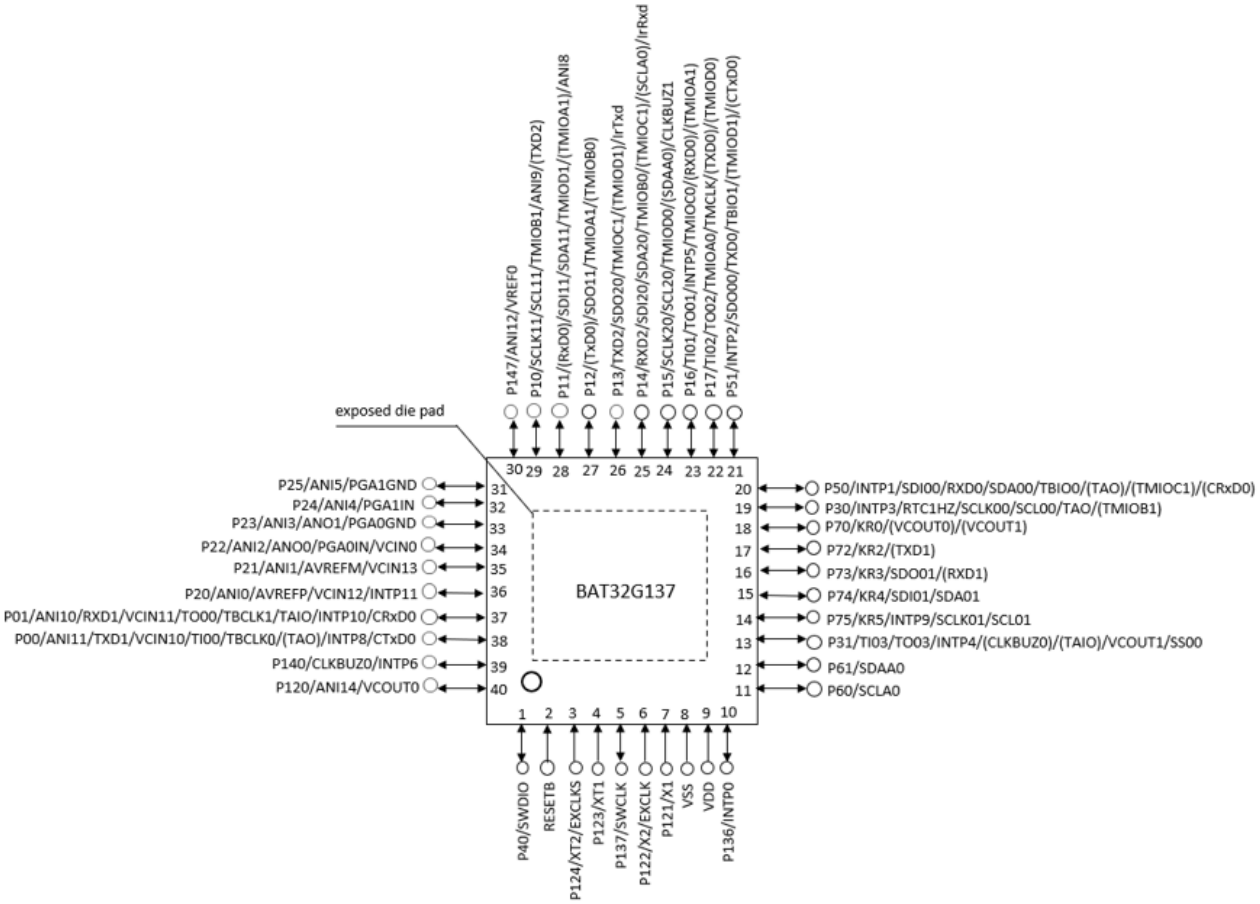
- 32LQFP（7x7mm, 0.8mm pitch）



Remark: Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register.

1.3.2 BAT32G137GH40NB

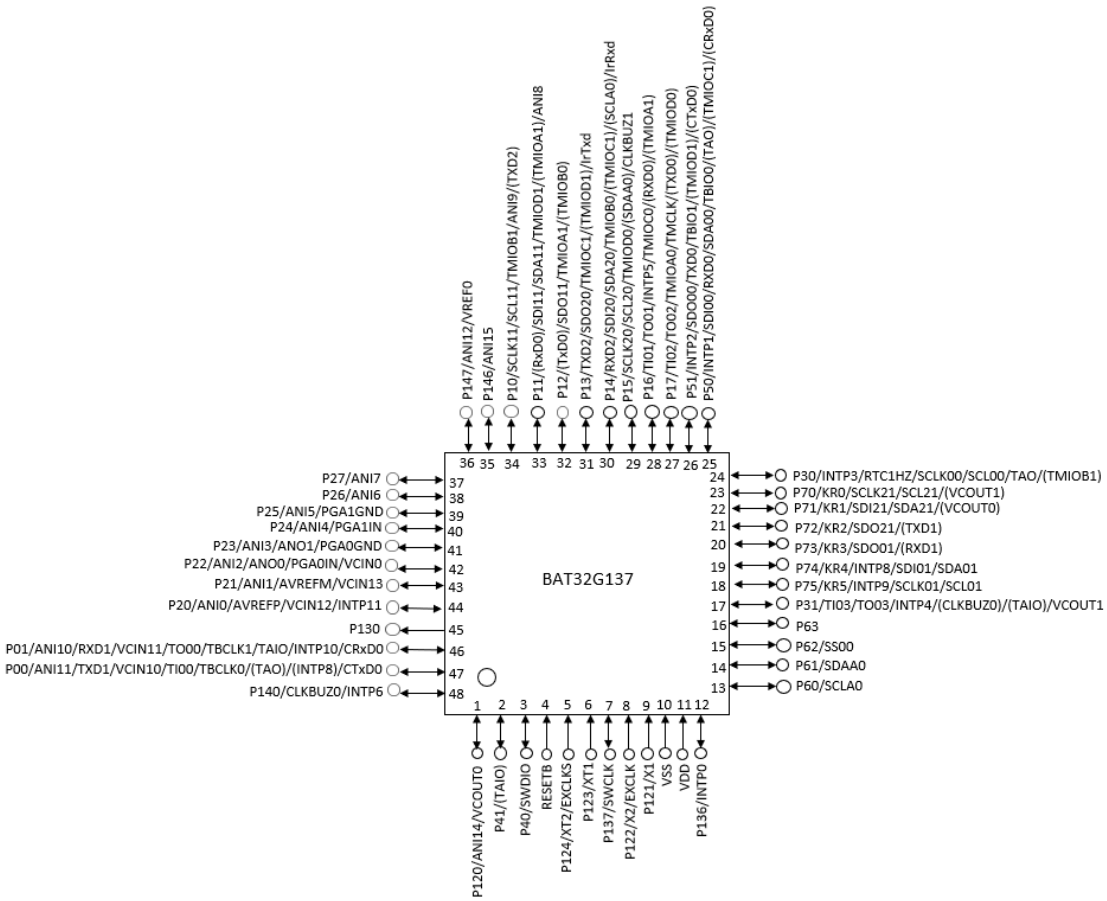
- 40QFN（5x5mm, 0.4mm pitch）



Remark:Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register.

1.3.3 BAT32G137GH48FA

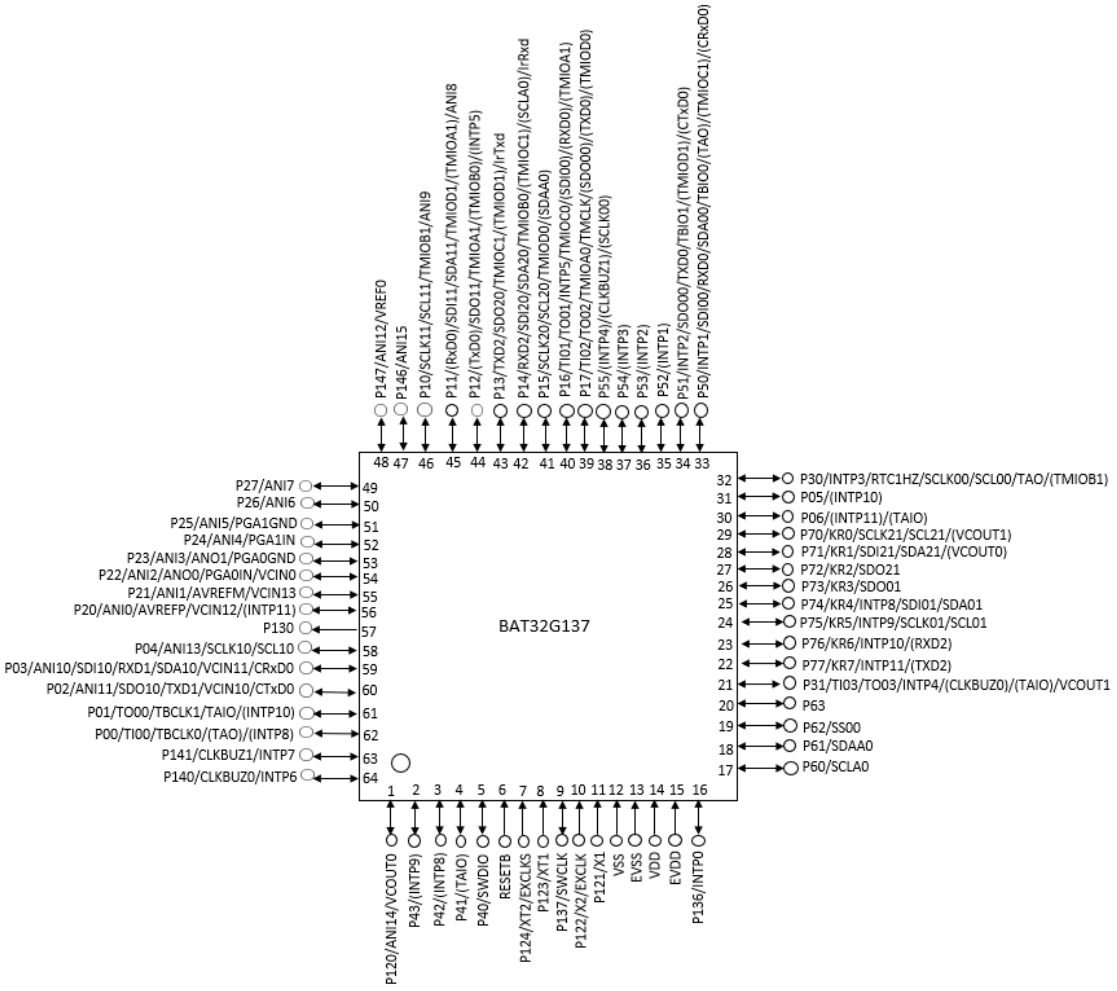
- 48LQFP（7x7mm, 0.5mm pitch）



Remark:Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register.

1.3.4 BAT32G137GH64FB

- 64LQFP（7x7mm, 0.4mm pitch）



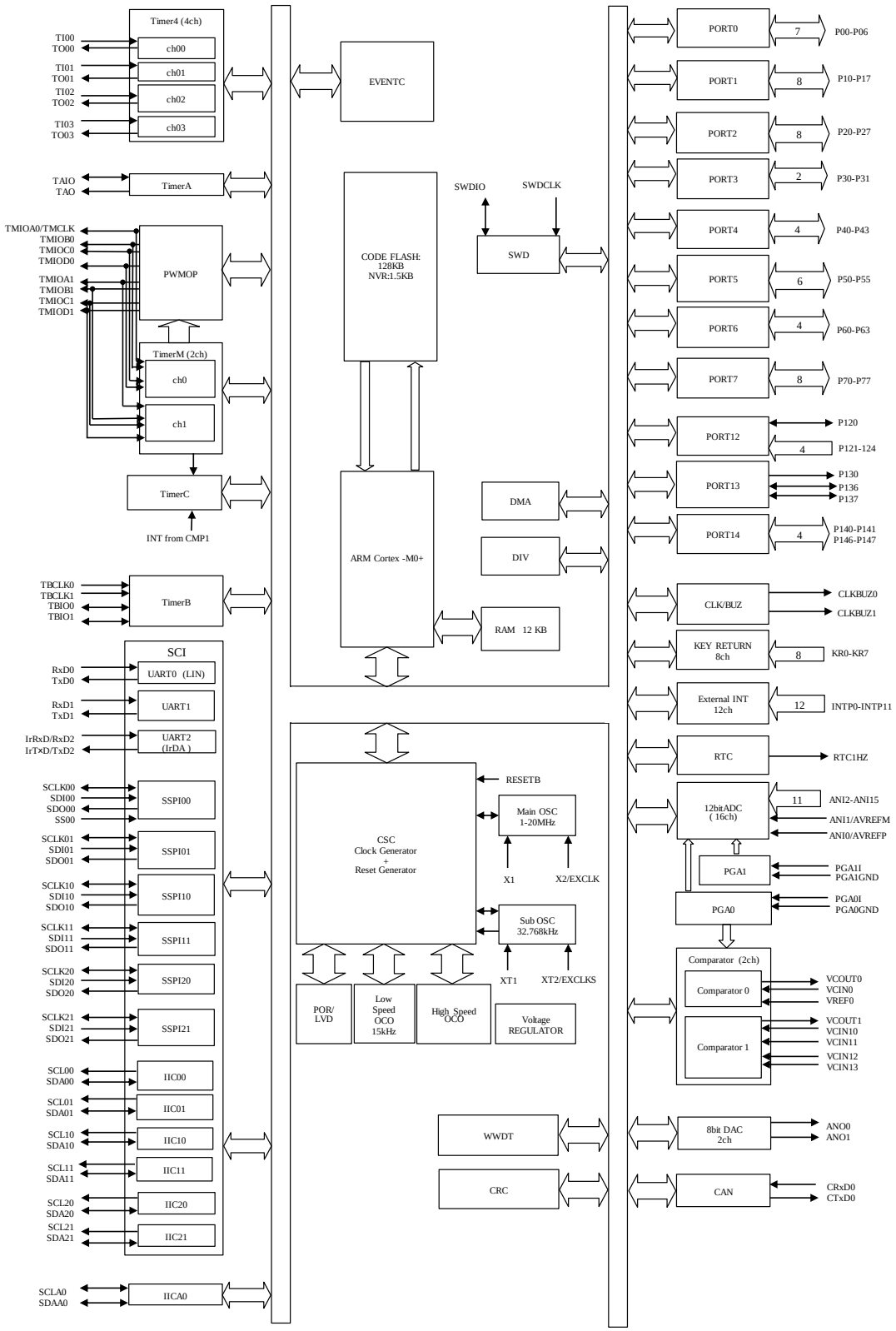
Caution 1. Make EVSS pin the same potential as VSS pin.

Caution 2. Make EVDD pin the same potential as VDD pin.

Remark 1. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD pins and connect the VSS and EVSS pins to separate ground lines.

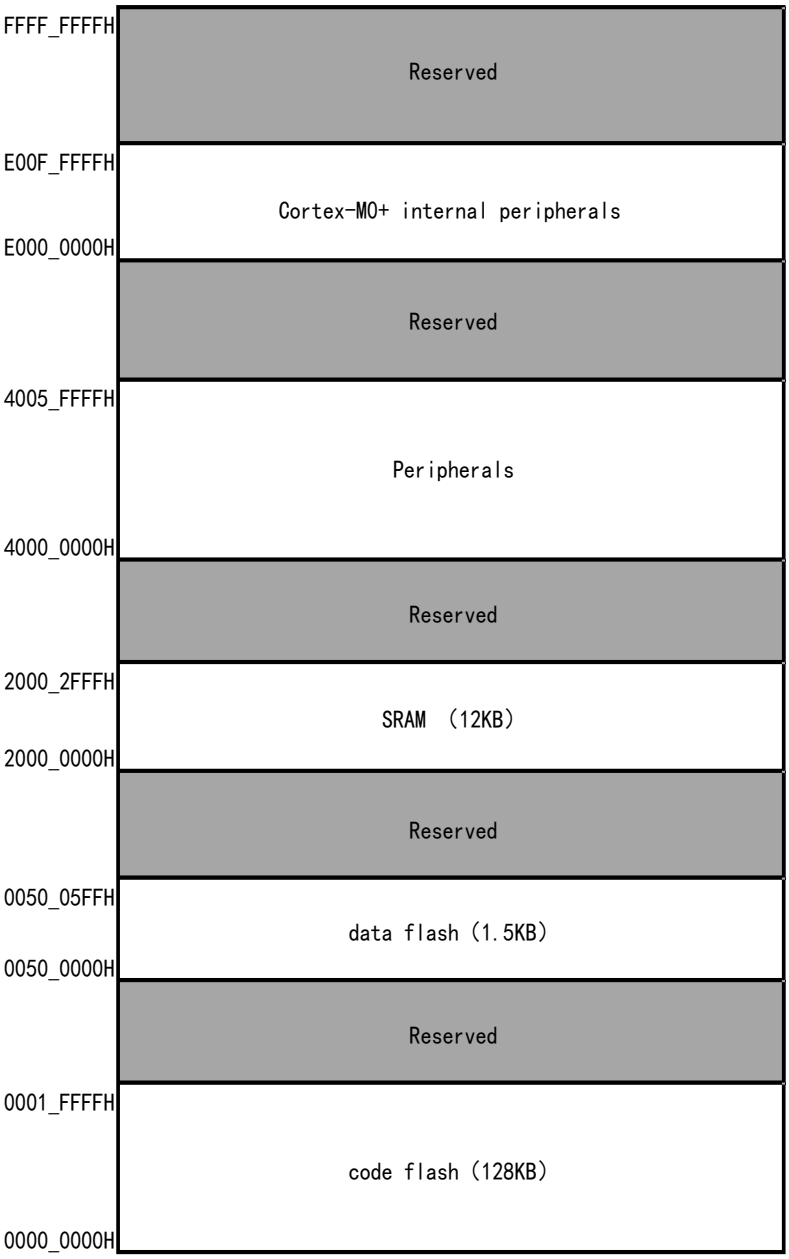
Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register.

2 Block Diagram



note: This is a block diagram of 64-pin products, some functions of products below 64 pins are not supported

3 Memory Space



4 PIN Funtions

4.1 Port Functions

Pin I/O buffer power supplies depend on the product. The relationship between these power supplies and the

pins are shown below.

64-pin product:

Power Supply	Corresponding Pins
EVDD/EVSS	Port pins other than P20～P27, P121～P124 , P137 and RESETB
VDD/VSS	P20～P27, P121～P124, P137 and RESETB

Products other than 64 pins use a single power supply, all pins are powered by VDD.

All ports of this product are divided into 5 types, from type 1 to type 5. The corresponding conditions are as follows:

Type 1: bidirectional I/O function

Type 2: NOD function, corresponding to pin P60-P63

Type 3: only input function, such as clock, corresponding to pin P121-P124

Type 4: only output function, corresponding to pin P130

Type 5: RESET function, corresponding to pin RESETB

See 4.3 Port Type for details of pin block diagram of each type

4.1.1 32-pin products

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Function Name	Port Type	I/O	After Reset Release	Alternate Function	Function
P00	Type1	I/O	Analog function	ANI11/TXD1/VCIN10/TI00/TBCLK0/(TAO)/INTP8/CTxD0	Port 0. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P01 can be set to TTL input buffer. Output of P00 can be set to N-ch open-drain output (VDD tolerance). P00 and P01 can be set to analog input
P01				ANI10/RXD1/VCIN11/TO00/TBCLK1/TAIO/INTP10/CRxD0	
P10		I/O	Analog function	SCLK11/SCL11/TMIOB1/ANI9/(TXD2)	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P10 and P14 to P17 can be set to TTL input buffer. Output of P10, P11, P13 to P15, and P17 can be set to N-ch open-drain output (VDD tolerance). P10 to P11 can be set to analog input.
P11				(RxD0)/SDI11/SDA11/TMIOD1/(TMIOA1)/ANI8	
P12			Input port	(TxD0)/SDO11/TMIOA1/(TMIOB0)	
P13				TxD2/SDO20/TMIOC1/(TMIOD1)/IrTxd	
P14				RxD2/SDI20/SDA20/TMIOB0/(TMIOC1)/(SCLA0)/IrRxd	
P15				SCLK20/SCL20/TMIOD0/(SDAA0)/CLKBUZ1	
P16				TI01/TO01/INTP5/TMIOC0/(RXD0)/(TMIOA1)	
P17				TI02/TO02/TMIOA0/TMCLK/(TXD0)/(TMIOD0)	
P20		I/O	Analog function	ANI0/AVREFP/VCIN12/(INTP11)	Port 2. 4-bit I/O port. Input/output can be specified in 1-bit units. Can be set to analog input.
P21				ANI1/AVREFM/VCIN13	
P22				ANI2/ANO0/PGA0IN/VCIN0	
P23				ANI3/ANO1/PGA0GND	
P30		I/O	Input port	INTP3/SCLK00/SCL00/TAO/(TMIOB1)	Port 3. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P30 and P31 can be set to TTL input buffer. Output of P30 and P31 can be set to N-ch Open-drain output (VDD tolerance).
P31				TI03/TO03/INTP4/CLKBUZ0/(TAIO)/VCOUT1/SS00/SCLA0	
P40		I/O	Input port	SWDIO	Port 4. 1-bit I/O port. Input/output can be specified. Use of an on-chip pull-up resistor can be specified by a software setting at input port.

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Function Name	Port Type	I/O	After Reset Release	Alternate Function	Function
P50	Type1	I/O	Input port	INTP1/SDI00/RXD0/SDA00/TBIO0/(TAO) /(TMIOC1) /(CRxD0)	Port 5. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P50 can be set to TTL input buffer. Output of P50 and P51 can be set to N-ch opendrain output (VDD tolerance).
P51				INTP2/SDO00/TXD0/TBIO1/(TMIOD1)/(CTxD0)	
P70	Type1	I/O	Input port	INTP6/(VCOUT1)	Port 7 The 4-bit input/output ports can be designated as inputs or outputs in bit units. The inputs can be set by software using internal pull-up resistors. The inputs of the P74 can be configured as TTL input buffers and the outputs can be configured as N-channel open-drain outputs (VDD withstand). The outputs of P71 and P74 can be set as N-channel open drain outputs (VDD withstand voltage).
P72				INTP7/(TXD1)	
P73				(RXD1)/(VCOUT0)	
P74		I/O	Input port	SDAA0	
P120		I/O	Analog function	ANI14/VCOUT0	Port 12. 1-bit I/O port and 2-bit input-only port. For only P120, input/output can be specified. For only P120, use of an on-chip pull-up resistor can be specified by a software setting at input port. P120 can be set to analog input.
P121	Typ3	I	Input port	X1	
P122				X2/EXCLK	
P136	Type1	I/O	Input port	INTP0	Port 13. 2-bit I/O port.
P137				SWCLK	
P147		I/O	Analog function	ANI12/VREF0	Port 14. 1-bit I/O port. Input/output can be specified. Use of an on-chip pull-up resistor can be specified by a software setting at input port. P147 can be set to analog input.
RESETB	Type5	I	—	—	Input-only pin for external reset. Connect to VDD directly or via a resistor when external reset is not used.

Note Each pin can be specified as either digital or analog by setting port mode control register x (PMCx) (Can be specified in 1-bit units).
Description of Alternate function,please refer to“4.2 pins other than port pins”.
Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register.

4.1.2 40-pin products

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Function Name	Port Type	I/O	After Reset Release	Alternate Function	Function
P00	Type1	I/O	Analog function	ANI11/TXD1/VCIN10/TI00/TBCLK0/(TAO) /INTP8/CTxD0	Port 0. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P01 can be set to TTL input buffer. Output of P00 can be set to N-ch open-drain output(VDD tolerance). P00 and P01 can be set to analog input
P01				ANI10/RXD1/VCIN11/TO00/TBCLK1 /TAIO/INTP10/CRxD0	
P10		I/O	Analog function	SCLK11/SCL11/TMIOB1/ANI9/(TXD2)	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P10 and P14 to P17 can be set to TTL input buffer. Output of P10, P11, P13 to P15, and P17 can be set to N-ch open-drain output (VDD tolerance). P10 to P11 can be set to analog input.
P11				(RxD0)/SDI11/SDA11/TMIOD1/(TMIOA1)/ANI 8	
P12			Input port	(TxD0)/SDO11/TMIOA1/(TMIOB0)	
P13				TxD2/SDO20/TMIOC1/(TMIOD1)/IrTxd	
P14				RxD2/SDI20/SDA20/ TMIOB0/(TMIOC1)/ (SCLA0)/IrRxd	
P15				SCLK20/SCL20/TMIOD0/(SDAA0)/CLK BUZ1	
P16				TI01/TO01/INTP5/TMIOC0/(RXD0)/(TMIO A1)	
P17				TI02/TO02/TMIOA0/TMCLK/(TXD0)/(TMIO D0)	
P20		I/O	Analog function	ANI0/AVREFP/VCIN12/(INTP11)	Port 2. 6-bit I/O port. Input/output can be specified in 1-bit units. Can be set to analog input.
P21				ANI1/AVREFM/VCIN13	
P22				ANI2/ANO0/PGA0IN/VCIN0	
P23				ANI3/ANO1/PGA0GND	
P24				ANI4/PGA1IN	
P25				ANI5/PGA1GND	
P30		I/O	Input port	INTP3/RTC1HZ/SCLK00/SCL00/TAO/(TMIO B1)	Port 3. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P30 can be set to TTL input buffer. Output of P30 can be set to N-ch open-drain output (VDD tolerance).
P31				TI03/TO03/INTP4/(CLKBUZ0)/ (TAIO)/VCOUT1/SS00	
P40		I/O	Input port	SWDIO	Port 4. 1-bit I/O port. Input/output can be specified. Use of an on-chip pull-up resistor can be specified by a software setting at input port.

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Function Name	Port Type	I/O	After Reset Release	Alternate Function	Function
P50	Type1	I/O	Input port	INTP1/SDI00/RXD0/SDA00/TBIO0/(TAO)	Port 5. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P50 can be set to TTL input buffer. Output of P50 and P51 can be set to N-ch open-drain output (VDD tolerance).
P51				INTP2/SDO00/TXD0/TBIO1/(TMIOD1)/(CTxD0)	
P60	Type2	I/O	Input port	SCLA0	Port 6. 2-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 and P61 is N-ch open-drain output (6 V tolerance).
P61				SDAA0	
P70	Type1	I/O	Input port	KR0/(VCOUT0)/(VCOUT1)	Port 7. 5-bit I/O port. Input/output can be specified. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Output of P74 can be set to N-ch open -drain output (VDD tolerance).
P72				KR2/(TXD1)	
P73				KR3/SDO01/(RXD1)	
P74				KR4/SDI01/SDA01	
P75				KR5/INTP9/SCLK01/SCL01	
P120		I/O	Analog function	ANI14/VCOUT0	Port 12. 1-bit I/O port and 2-bit input-only port. For only P120, input/output can be specified. For only P120, use of an on-chip pull-up resistor can be specified by a software setting at input port. P120 can be set to analog input.
P121	Type3	I	Input port	X1	
P122				X2/EXCLK	
P123				XT1	
P124				XT2/EXCLKS	
P136	Type1	I/O	Input port	INTP0	Port 13. 2-bit I/O port.
P137				SWCLK	
P140		I/O	Input port	CLKBUZ0/INTP6	Port 14. 2-bit I/O port. Input/output can be specified. Use of an on-chip pull-up resistor can be specified by a software setting at input port. P147 can be set to analog input.
P147			Analog function	ANI12/VREF0	
RESETB	Type5	I	—	—	Input-only pin for external reset. Connect to VDD directly or via a resistor When external reset is not used.

Note Each pin can be specified as either digital or analog by setting port mode control register x (PMCx) (Can be specified in 1-bit units).

Description of Alternate function,please refer to“4.2 pins other than port pins”.

Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register.

4.1.3 48-pin products

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Function Name	Port Type	I/O	After Reset Release	Alternate Function	Function
P00	Type1	I/O	Analog function	ANI11/TXD1/VCIN10/TI00/TBCLK0/(TAO)/(INTP8)/CTxD0	Port 0. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P01 can be set to TTL input buffer. Output of P00 can be set to N-ch open-drain output(VDD tolerance). P00 and P01 can be set to analog input
P01				ANI10/RXD1/VCIN11/TO00/TBCLK1/TAIO/INTP10/CRxD0	
P10		I/O	Analog function	SCLK11/SCL11/TMIOB1/ANI9/(TXD2)	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P10 and P14 to P17 can be set to TTL input buffer. Output of P10, P11, P13 to P15, and P17 can be set to N-ch open-drain output (VDD tolerance). P10 to P11 can be set to analog input.
P11				(RxD0)/SDI11/SDA11/TMIOD1/(TMIOA1)/ANI8	
P12			Input port	(TxD0)/SDO11/TMIOA1/(TMIOB0)	
P13				TxD2/SDO20/TMIOC1/(TMIOD1)/IrTxd	
P14				RxD2/SDI20/SDA20/ TMIOB0/(TMIOC1)/(SCLA0)/IrRxd	
P15				SCLK20/SCL20/TMIOD0/(SDAA0)/CLKBUZ1	
P16				TI01/TO01/INTP5/TMIOC0/(RXD0)/(TMIOA1)	
P17				TI02/TO02/TMIOA0/TMCLK/(TXD0)/(TMIOD0)	
P20		I/O	Analog function	ANI0/AVREFP/VCIN12/INTP11	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units. Can be set to analog input.
P21				ANI1/AVREFM/VCIN13	
P22				ANI2/ANO0/PGA0IN/VCIN0	
P23				ANI3/ANO1/PGA0GND	
P24				ANI4/PGA1IN	
P25				ANI5/PGA1GND	
P26				ANI6	
P27				ANI7	
P30		I/O	Input port	INTP3/RTC1HZ/SCLK00/SCL00/TAO/(TMIOB1)	Port 3. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P30 can be set to TTL input buffer. Output of P30 can be set to N-ch open-drain output (VDD tolerance).
P31				TI03/TO03/INTP4/(CLKBUZ0)/(TAIO)/VCOUT1	
P40		I/O	Input port	SWDIO	Port 4. 2-bit I/O port. Input/output can be specified. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P41				(TAIO)	

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Function Name	Port Type	I/O	After Reset Release	Alternate Function	Function
P50	Type1	I/O	Input port	INTP1/SDI00/RXD0/SDA00/TBIO0/(TAO) /(TMIOC1)/(CRxD0)	Port 5. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P50 can be set to TTL input buffer. Output of P50 and P51 can be set to N-ch open-drain output (VDD tolerance).
P51				INTP2/SDO00/TXD0/TBIO1/(TMIOD1)/(CTxD0)	
P60	Type2	I/O	Input port	SCLA0	Port 6. 4-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 and P63 is N-ch open-drain output (6 V tolerance).
P61				SDAA0	
P62				SS00	
P63				—	
P70	Type1	I/O	Input port	KR0/SCLK21/SCL21/(VCOUT1)	Port 7. 6-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Output of P71 and P74 can be set to N-ch open-drain output (VDD tolerance).
P71				KR1/SDI21/SDA21/(VCOUT0)	
P72				KR2/SDO21/(TXD1)	
P73				KR3/SDO01/(RXD1)	
P74				KR4/INTP8/SDI01/SDA01	
P75				KR5/INTP9/SCLK01/SCL01	
P120		I/O	Analog function	ANI14/VCOUT0	Port 12. 1-bit I/O port and 2-bit input-only port. For only P120, input/output can be specified. For only P120, use of an on-chip pull-up resistor can be specified by a software setting at input port. P120 can be set to analog input.
P121	Type3	I	Input port	X1	
P122				X2/EXCLK	
P123				XT1	
P124				XT2/EXCLKS	
P130	Type4	O	Output port	—	Port 13. 1-bit output-only port and 2-bit I/O port.
P136	Type1	I/O	Input port	INTP0	
P137				SWCLK	
P140		I/O	Input port	CLKBUZ0/INTP6	Port 14. 3-bit I/O port. Input/output can be specified. Use of an on-chip pull-up resistor can be specified by a software setting at input port. P146 and P147 can be set to analog input.
P146			Analog function	ANI15	
P147				ANI12/VREF0	
RESETB	Type5	I	—	—	Input-only pin for external reset. Connect to VDD directly or via a resistor when external reset is not used.

Note Each pin can be specified as either digital or analog by setting port mode control register x (PMCx) (Can be specified in 1-bit units).
Description of Alternate function,please refer to“4.2 pins other than port pins”.
Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register.

4.1.4 64-pin products

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Function Name	Port Type	I/O	After Reset Release	Alternate Function	Function
P00	Type1	I/O	Input port	TI00/TBCLK0/(TAO)/(INTP8)	Port 0. 7-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P01, P03 and P04 can be set to TTL input buffer. Output of P00 and P02 to P04 can be set to N-ch open-drain output (EVDD tolerance). P02, P03 and P04 can be set to analog input.
P01				TO00/TBCLK1/TAIO/(INTP10)	
P02			Analog function	ANI11/SDO10/TXD1/VCIN10/CTxD0	
P03				ANI10/SDI10/RXD1/SDA10/VCIN11/CRxD0	
P04				ANI13/SCLK10/SCL10	
P05			Input port	(INTP10)	
P06				(INTP11)/(TAIO)	
P10		I/O	Analog function	SCLK11/SCL11/TMIOB1/ANI9	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P10 and P14 to P17 can be set to TTL input buffer. Output of P10, P11, P13 to P15, and P17 can be set to N-ch open-drain output (EVDD tolerance). P10 to P11 can be set to analog input.
P11				(RxD0)/SDI11/SDA11/TMIOD1/(TMIOA1)/ANI8	
P12			Input port	(TxD0)/SDO11/TMIOA1/(TMIOB0)/(INTP5)	
P13				TXD2/SDO20/TMIOC1/(TMIOD1)/IrTxd	
P14				RXD2/SDI20/SDA20/TMIOB0/(TMIOC1)/(SCLA0)/IrRxd	
P15				SCLK20/SCL20/TMIOD0/ (SDAA0)	
P16				TI01/TO01/INTP5/TMIOC0/(SDI00)/(RXD0)/(TMIOA1)	
P17				TI02/TO02/TMIOA0/TMCLK/(SDO00)/(TXD0)/(TMIOD0)	
P20		I/O	Analog function	ANI0/AVREFP/VCIN12/(INTP11)	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units. Can be set to analog input.
P21				ANI1/AVREFM/VCIN13	
P22				ANI2/ANO0/PGA0IN/VCIN0	
P23				ANI3/ANO1/PGA0GND	
P24				ANI4/PGA1IN	
P25				ANI5/PGA1GND	
P26				ANI6	
P27				ANI7	
P30		I/O	Input port	INTP3/RTC1HZ/SCLK00/SCL00/TAO/(TMIOB1)	Port 3. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P30 can be set to TTL input buffer. Output of P30 can be set to N-ch open-drain output (EVDD tolerance).
P31				TI03/TO03/INTP4/(CLKBUZ0)/(TAIO)/VCOUT1	

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Function Name	Port Type	I/O	After Reset Release	Alternate Function	Function
P40	Type1	I/O	Input port	SWDIO	Port 4. 4-bit I/O port. Input/output can be specified. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P41				(TAIO)	
P42				(INTP8)	
P43				(INTP9)	
P50		I/O	Input port	INTP1/SDI00/RXD0/SDA00/TBIO0/(TAO)/(TMIOC1)/(CRxD0)	Port 5. 6-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P50 and P55 can be set to TTL input buffer. Output of P50, P51, and P55 can be set to N-ch open-drain output (EVDD tolerance).
P51				INTP2/SDO00/TXD0/TBIO1/(TMIOD1)/(CTxD0)	
P52				(INTP1)	
P53				(INTP2)	
P54				(INTP3)	
P55				(INTP4)/(CLKBUZ1)/(SCLK00)	
P60	Type2	I/O	Input port	SCLA0	Port 6. 4-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 and P63 is N-ch open-drain output (6 V tolerance).
P61				SDAA0	
P62				SS00	
P63				—	
P70	Type1	I/O	Input port	KR0/SCLK21/SCL21/(VCOUT1)	Port 7. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Output of P71 and P74 can be set to N-ch open-drain output (EVDD tolerance).
P71				KR1/SDI21/SDA21/(VCOUT0)	
P72				KR2/SDO21	
P73				KR3/SDO01	
P74				KR4/INTP8/SDI01/SDA01	
P75				KR5/INTP9/SCLK01/SCL01	
P76				KR6/INTP10/(RxD2)	
P77				KR7/INTP11/(TxD2)	
P120		I/O	Analog function	ANI14/VCOUT0	Port 12. 1-bit I/O port and 2-bit input-only port. For only P120, input/output can be specified. For only P120, use of an on-chip pull-up resistor can be specified by a software setting at input port. P120 can be set to analog input.
P121	Type3	I	Input port	X1	
P122				X2/EXCLK	
P123				XT1	
P124				XT2/EXCLKS	
P130	Type4	O	Output port	—	Port 13. 1-bit output-only port and 2-bit I/O port.
P136	Type1	I/O	Input port	INTP0	
P137				SWCLK	
P140		I/O	Input port	CLKBUZ0/INTP6	Port 14. 3-bit I/O port. Input/output can be specified. Use of an on-chip pull-up resistor can be specified by a software setting at input port. P146 and P147 can be set to analog input.
P141				CLKBUZ1/INTP7	
P146			Analog function	ANI15	
P147				ANI12/VREF0	
RESETB	Type5	I	—	—	Input-only pin for external reset. Connect to VDD directly or via a resistor when external reset is not used.

Note Each pin can be specified as either digital or analog by setting port mode control register x (PMCx) (Can be specified in 1-bit units).
Description of Alternate function,please refer to“4.2 pins other than port pins”.
Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register.

4.2 pins other than port pins

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Function Name	I/O	Function
ANI0 ~ ANI15	I	A/D converter analog input
ANO0, ANO1	O	D/A converter output
INTP0 ~ INTP11	I	External interrupt request input pin for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.
VCIN0	I	Comparator 0 analog voltage input
VCIN10, VCIN11, VCIN12, VCIN13	I	Comparator 1 analog voltage input/reference voltage input
VREF0	I	Comparator 0 reference voltage input
VCOUT0, VCOUT1	O	Comparator output
PGA0IN, PGA1IN	I	PGA voltage input
PGA0GND, PGA1GND	I	PGA reference voltage input
KR0 ~ KR7	I	Key interrupt input
CLKBUZ0, CLKBUZ1	O	Clock output/buzzer output
RTC1HZ	O	Real-time clock correction clock (1Hz) output
RESETB	I	This is the active-low system reset input pin. When the external reset pin is not used, connect this pin directly or via a resistor to VDD.
CRxD0	I	CAN receive data
CTxD0	O	CAN transmit data
IrRxD	I	IrDA receive data
IrTxD	O	IrDA transmit data
RxD0 ~ RxD2	I	Serial data input pins of serial interface UART0 to UART2
TxD0 ~ TxD2	O	Serial data output pins of serial interface UART0 to UART2
SCL00, SCL01, SCL10, SCL11, SCL20, SCL21	O	Serial clock output pins of serial interface IIC00, IIC01, IIC10, IIC11, IIC20, and IIC21
SDA00, SDA01, SDA10, SDA11, SDA20, SDA21	I/O	Serial data I/O pins of serial interface IIC00, IIC01, IIC10, IIC11, IIC20, and IIC21
SCLK00, SCLK01, SCLK10, SCLK11, SCLK20, SCLK21	I/O	Serial clock I/O pins of serial interface SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, and SSPI21
SDI00, SDI01, SDI10, SDI11, SDI20, SDI21	I	Serial data input pins of serial interface SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, and SSPI21

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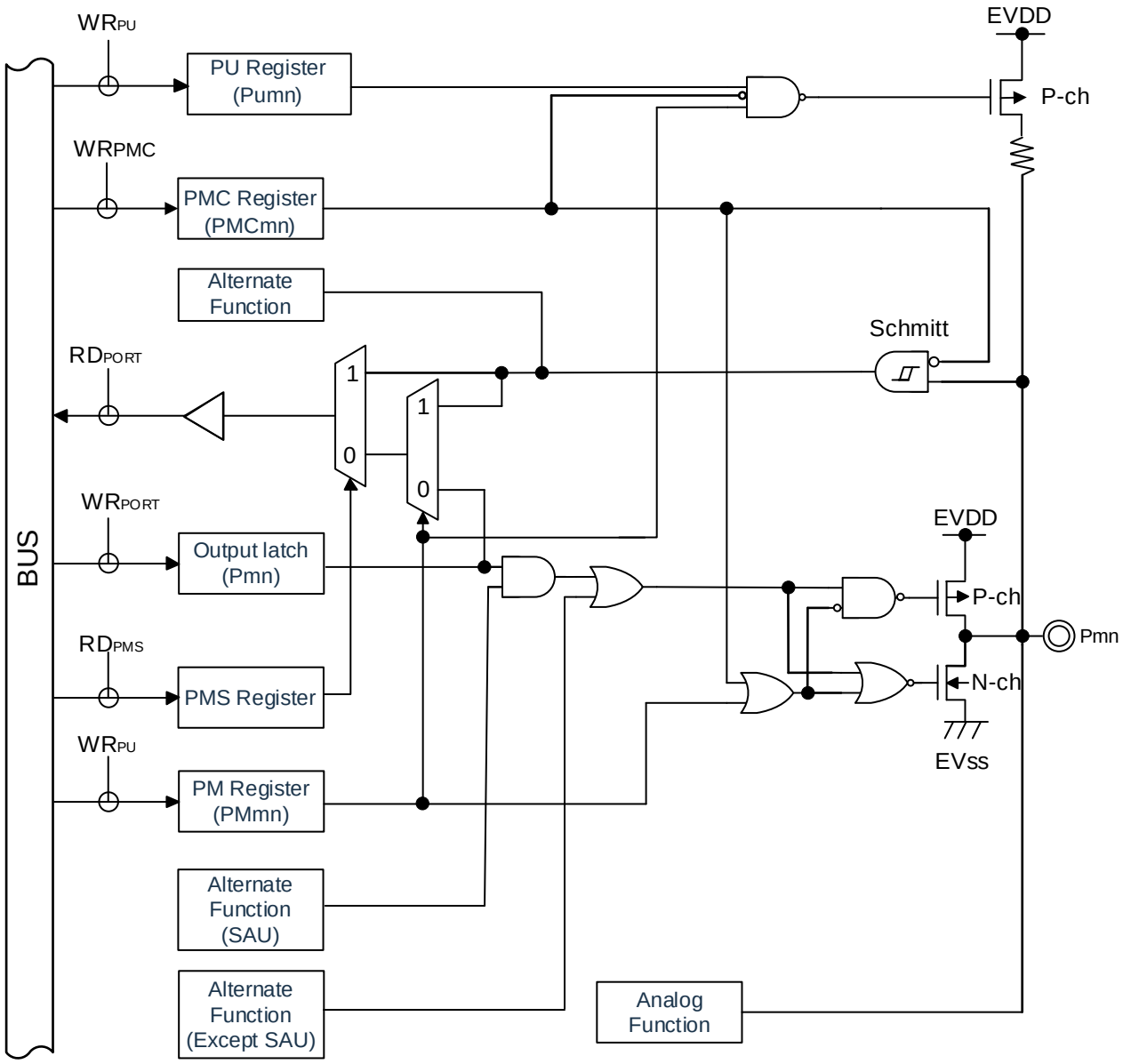
Function Name	I/O	Function
SS00	I	Chip select input pin of serial interface SSPI00
SDO00, SDO01, SDO10, SDO11, SDO20, SDO21	O	Serial data output pins of serial interface SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, and SSPI21
SCLA0	I/O	Serial clock I/O pins of serial interface IICA0
SDAA0	I/O	Serial data I/O pins of serial interface IICA0
TI00 ~ TI03	I	The pins for inputting an external count clock/capture trigger to 16-bit Timer4
TO00 ~ TO03	O	Timer output pins of 16-bit Timer4
TAIO	I/O	TimerA input/output
TAO	O	TimerA output
TMCLK	I	TimerM external clock input
TMIOA0, TMIOB0, TMIOC0, TMIOD0, TMIOA1, TMIOB1, TMIOC1, TMIOD1	I/O	TimerM input/output
TBIO0, TBIO1	I/O	TimerB input/output
TBCLK0, TBCLK1	I	TimerB external clock input
X1, X2	—	Resonator connection for main system clock
EXCLK	I	External clock input for main system clock
XT1, XT2	—	Resonator connection for subsystem clock
EXCLKS	I	External clock input for subsystem clock
VDD	—	＜32-pin, 40-pin, 48-pin＞: Positive power supply for all pins ＜64-pin＞:Positive power supply for P20～P27, P121～P124, P137 and RESETB
EVDD	—	Positive power supply for ports (other than P20 to P27, P121 to P124, P137 and RESETB)
AVREFP	I	A/D converter reference potential (+ side) input
AVREFM	I	A/D converter reference potential (- side) input
VSS	—	＜32-pin, 40-pin, 48-pin＞: Ground potential for all pins ＜64-pin＞:Ground potential for P20～P27, P121～P124, P137 and RESETB
EVSS	—	Ground potential for ports (other than P20 to P27, P121 to P124, P137 and RESETB)
SWDIO	I/O	SWD data line
SWCLK	I	SWD clock line

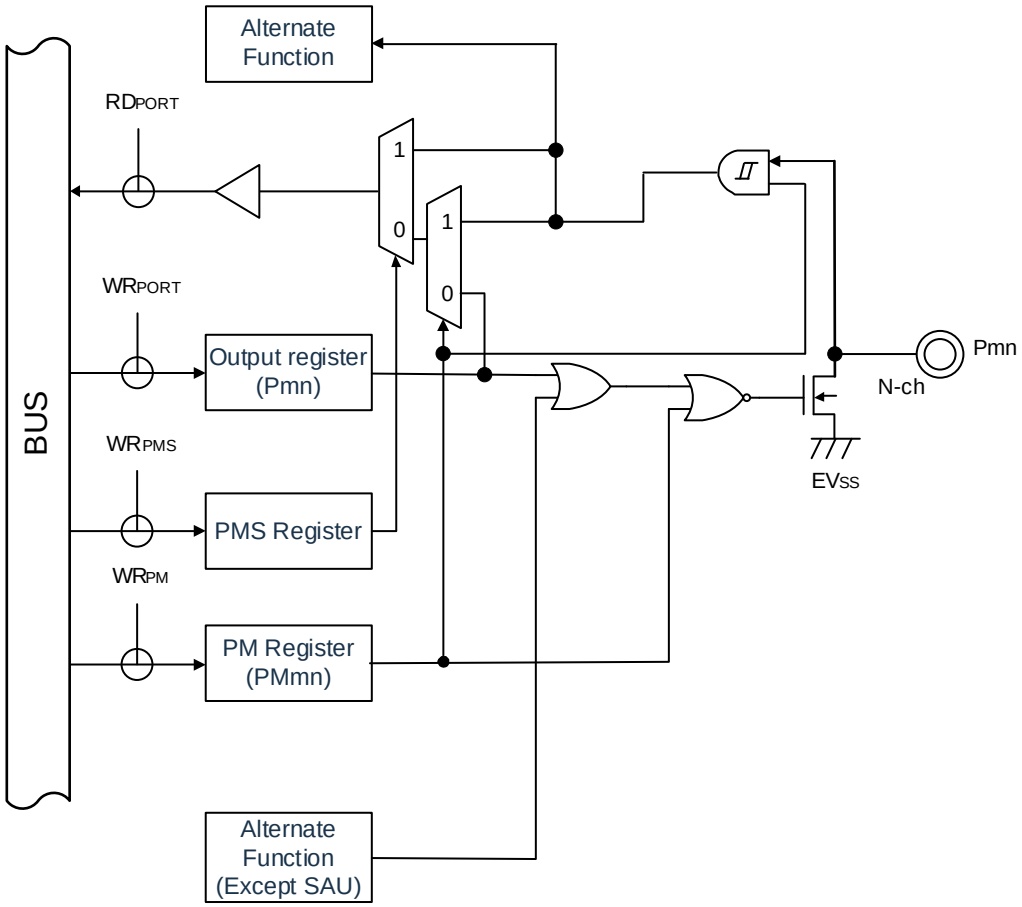
Remark Use bypass capacitors (about 0.1 uF) as noise and latch up countermeasures with relatively thick wires at the shortest distance to V_{DD} to V_{SS} and EV_{DD} to EV_{SS} lines.

4.3 Port Type

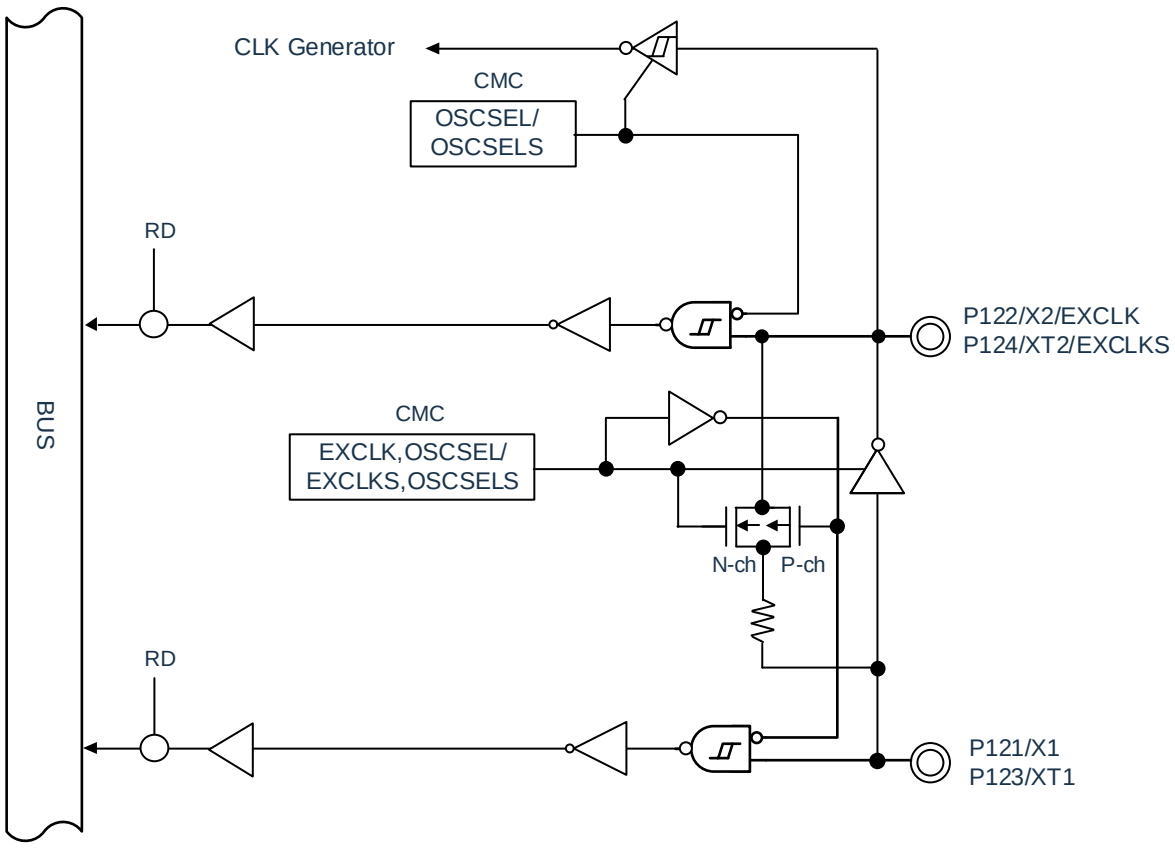
Type 1: Dual I/O function



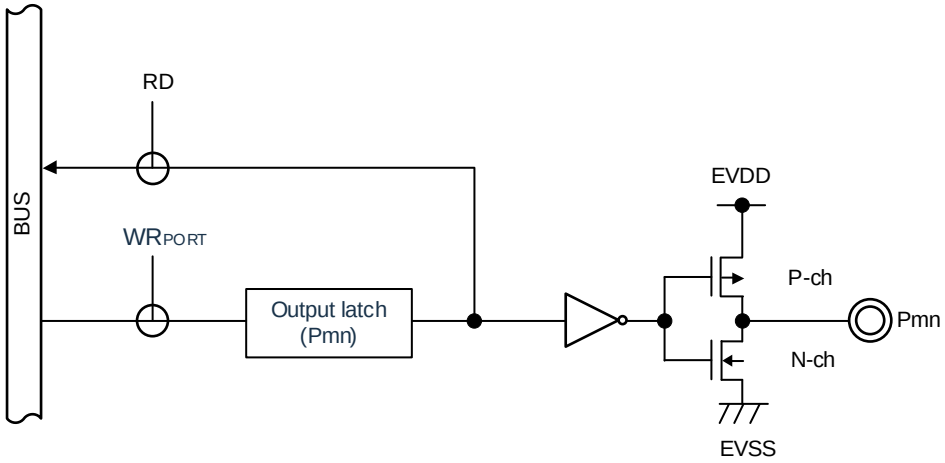
Type 2：NOD function



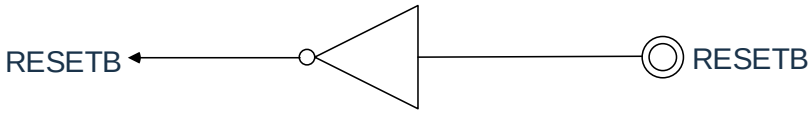
Type 3: input function only



Type 4: output function only



Type 5: RESET function



5 Functional Overview

5.1 ARM® Cortex®-M0+ core with MPU

Cortex-M0(+) processor is a new generation of ARM processors for embedded systems. It provides a low-cost platform for low pin count and low power consumption microcontrollers, while providing excellent computing performance and advanced system response to interrupts.

The 32-bit RISC processor of the Cortex-M0(+) processor provides excellent code efficiency and provides high-performance expectations of the ARM core, which is different from 8-bit and 16-bit devices of the same memory size. The Cortex-M0(+) processor has 32 address lines and a storage space of up to 4G.

The Cortex-M0(+) processor equipped with this product integrates the MPU memory protection unit: provides hardware management and protection of memory, and controls access rights.

BAT32G137 uses an embedded ARM core, so it is compatible with all ARM tools and software.

5.2 Memory

5.2.1 Flash

Function introduction:

- 128KB Flash Memory(program/data flash).
- 1.5 KB Special data flash memory
- Support sector erase, sector size is 512byte, erase time 4ms
- Support byte/half-word/word (32bit) programming, programming time 24us

5.2.2 SRAM

The MCU provides an on-chip high-speed SRAM module of 12KB with either parity-bit checking.

5.3 DMA

The built-in DMA (Direct Memory Access) controller can realize the function of data transfer between memories without using the CPU.

- Support the start of DMA through the interruption of peripheral functions, which can realize real-time control through communication, timer and A/D.
- Transfer space: 4 GB area from 0000 0000h to FFFF FFFFh except reserved areas.
- Support 4 transfer modes (normal transfer mode, repeat transfer mode, block transfer mode and chain transfer mode).

5.4 Event Link Controller (EVENTC)

The Event Link Controller (EVENTC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention.

The EVENTC has the following functions:

- Capable of directly linking event signals from 22 types of peripheral functions to specified peripheral functions.
- Event signals can be used as activation sources for operating any one of 10 types of peripheral functions.

5.5 Clock Generator

The clock generator generates the clock to be supplied to the CPU and peripheral hardware.

The following three kinds of system clocks and clock oscillators are selectable.

5.5.1 Main system clock

- X1 oscillator:
  This circuit oscillates a clock of fX = 1 to 20 MHz by connecting a resonator to X1 pin and X2 pin.
  Oscillation can be stopped by executing the DEEPSLEEP instruction or setting of the MSTOP bit.
- High-speed on-chip oscillator (High-speed OCO):
  The frequency at which to oscillate can be selected from among fHOCO = 64, 48, 32, 24, 16, 12, 8, 6,4, 3, 2, or 1 MHz (TYP.) by using the option byte.After a reset release, the CPU always starts operating with this high-speed on-chip oscillator clock. Oscillation can be stopped by executing the DEEPSLEEP instruction or setting of the HIOSTOP bit. The frequency specified by using an option byte can be changed by using the high-speed on-chip oscillator frequency select register (HOCODIV).
- X2 external main system clock:
  An external main system clock (fEX = 1 to 20 MHz) can also be supplied from the EXCLK/X2/P122 pin.
  An external main system clock input can be disabled by executing the STOP instruction or setting of the MSTOP bit.

5.5.2 Subsystem clock

- XT1 clock oscillator:
  This circuit oscillates a clock of fXT = 32.768 kHz by connecting a 32.768 kHz resonator to XT1 pin and XT2 pin.Oscillation can be stopped by setting the XTSTOP bit.
- XT2 external subsystem clock:
  An external subsystem clock (fEXS = 32.768 kHz) can also be supplied from the EXCLKS/XT2/P124 pin.
  An external subsystem clock input can be disabled by the setting of the XTSTOP bit.

5.5.3 Low-speed on-chip oscillator

- Low-speed on-chip oscillator (Low-speed OCO):

  This circuit oscillates a clock of fIL = 15 kHz (TYP.).

  The low-speed on-chip oscillator clock cannot be used as the CPU clock.

  Only the following peripheral hardware runs on the low-speed on-chip oscillator clock.
  - Watchdog timer（WWDT）
  - Real-time clock（RTC）
  - 15-bit interval timer
  - timerA

5.6 Power Management

5.6.1 Power supply

VDD :External power, voltage range 2.0 to 5.5V
EVDD :External I/O power, voltage range 2.0 to 5.5V
Make EVDD pin the same potential as VDD pin.

5.6.2 Power-on-reset circuit

The power-on-reset circuit (POR) has the following functions.

- Generates internal reset signal at power on. The reset signal is released when the supply voltage (VDD) exceeds the detection voltage (VPOR). Note that the reset state must be retained until the operating voltage becomes in the range defined of POR function. This can be achieved by utilizing the voltage detection circuit or controlling the externally input reset signal.
- Compares supply voltage (VDD) and detection voltage (VPDR), and then generates internal reset signal when VDD < VPDR. Note that, after power is supplied, this LSI should be placed in the DEEPSLEEP mode, or in the reset state by utilizing the voltage detector or externally input reset signal, before the operation voltage falls below the range defined of POR function. When restarting the operation, make sure that the operation voltage has returned within the range of operation.

5.6.3 Voltage detector

The operation mode and detection voltages (VLVDH, VLVDL, VLVD) for the voltage detector is set by using the option byte . The voltage detector (LVD) has the following functions.

- The LVD circuit compares the supply voltage (VDD) with the detection voltage (VLVDH, VLVDL, VLVD), and generates an internal reset or internal interrupt signal.
- The detection level for the power supply detection voltage (VLVDH, VLVDL) can be selected by using the option byte as one of 10 levels.
- Operable in DEEPSLEEP mode.
- When the power supply rises, before reaching the working voltage range, it must be kept in the reset state through the voltage detection circuit or external reset. When the power supply drops, it must be transferred to deep sleep mode before it is less than the operating voltage range, or set to the reset state by the voltage detection circuit or external reset.
- The range of operating voltage varies with the setting of the user option byte.

5.7 Low Power Modes

The product supports two low-power modes with short start-up time::

- SLEEP Mode:When a WFI instruction is executed while SBYCR.SSBY bit is 0, the MCU enters Sleep mode. In this mode, the CPU stops operating but the contents of its internal registers are retained. Other peripheral functions do not stop. Available resets or interrupts in Sleep mode cause the MCU to cancel Sleep mode.
- DEEPSLEEP Mode:When a WFI instruction is executed while SBYCR.SSBY bit is 1, the MCU enters Software Deepsleep mode. In this mode,the CPU, most of the on-chip peripheral functions and oscillators stop. However, the contents of the CPU internal registers and SRAM data, the states of on-chip peripheral functions and the I/O Ports are retained. Deepsleep mode allows a significant reduction in power consumption because most of the oscillators stop in this mode.

In either mode, the registers, flags, and data memory retain their contents before being set to standby mode, and also maintain the status of the output latch and output buffer of the input/output port.

5.8 Reset Function

The following seven operations are available to generate a reset signal.

(1) External reset input via RESETB pin

(2) Internal reset by watchdog timer program loop detection

(3) Internal reset by comparison of supply voltage and detection voltage of power-on-reset (POR) circuit

(4) Internal reset by comparison of supply voltage of the voltage detector (LVD) and detection voltage

(5) Internal reset by RAM parity error

(6) Internal reset by illegal-memory access

(7) software reset

External and internal resets start program execution from the address at 0000H and 0001H when the reset signal is generated.

5.9 Interrupts

The Cortex-M0+ processor has a built-in Nested Vectored Interrupt Controller (NVIC) that supports up to 32 interrupt request (IRQ) inputs and one non-maskable interrupt (NMI) input. In addition, the processor supports multiple internal exceptions.

This product extends 32 maskable interrupt requests (IRQ) and 1 non-maskable interrupt (NMI), and can support up to 64 maskable interrupt sources and one non-maskable interrupt source. The actual number of interrupt sources varies by product.

5.10 Real-timer Clock (RTC)

The real-time clock has the following features.

- Counters of year, month, week, day, hour, minute, and second.
- Constant-period interrupt function (period: 0.5 seconds, 1 second, 1 minute, 1 hour, 1 day, 1 month)
- Alarm interrupt function (alarm: week, hour, minute)
- Pin output function of 1 Hz
- Support frequency division of sub-system clock or main system clock as RTC running clock
- Real-time clock interrupt signal (INTRTC) can be used to wake up in deep sleep mode
- Support a wide range of clock correction functions

Caution: The count of year, month, week, day, hour, minutes and second can only be performed when a subsystem clock (f_{SUB} = 32.768 kHz) is selected as the operation clock of the real-time clock. When the low-speed oscillation clock (f_{IL} = 15 kHz) is selected, only the constant-period interrupt function is available.

5.11 Watchdog Timer

The counting operation of the watchdog timer is set by the option byte. The watchdog timer operates on the low-speed on-chip oscillator clock (fIL). The watchdog timer is used to detect an inadvertent program loop. If a program loop is detected, an internal reset signal is generated.

Program loop is detected in the following cases:

- If the watchdog timer counter overflows
- If a 1-bit manipulation instruction is executed on the watchdog timer enable register (WDTE)
- If data other than “ACH” is written to the WDTE register
- If data is written to the WDTE register during a window close period

5.12 SysTick Timer

This timer is dedicated to real-time operating systems, but can also be used as a standard down counter.

Its characteristics are: when the 24-bit down counter self-loading capacity counter reaches 0, there is a shieldable system interruption.

5.13 timer4

The timer array unit has four 16-bit timers. Each 16-bit timer is called a channel and can be used as an independent timer. In addition, two or more “channels” can be used to create a high-accuracy timer.

For details about each function, see the table below.

Independent channel operation function	Simultaneous channel operation function
●Interval timer ●Square wave output (●External event counter ●Divider ●Input pulse interval measurement ●Measurement of high-/low-level width of input signal ●Delay counter	●One-shot pulse output ●PWM output ●Multiple PWM output

5.13.1 Independent channel operation function

By operating a channel independently, it can be used for the following purposes without being affected by the operation mode of other channels.

(1) Interval timer: Each timer of the unit can be used as a reference timer that generates an interrupt (INTTM) at fixed intervals.

(2) Square wave output: A toggle operation is performed each time INTTMmn interrupt is generated and a square wave with a duty factor of 50% is output from a timer output pin (TO).

(3) External event counter: Each timer of the unit can be used as an event counter that generates an interrupt when the number of the valid edges of a signal input to the timer input pin (TI) has reached a specific value.

(4) Divider function (channel 0 only): A clock input from a timer input pin (TI00) is divided and output from an output pin (TO00).

(5) Input pulse interval measurement: Counting is started by the valid edge of a pulse signal input to a timer input pin (TI). The count value of the timer is captured at the valid edge of the next pulse. In this way, the interval of the input pulse can be measured.

(6) Measurement of high-/low-level width of input signal: Counting is started by a single edge of the signal input to the timer input pin (TI), and the count value is captured at the other edge. In this way, the high-level or low-level width of the input signal can be measured.

(7) Delay counter: Counting is started at the valid edge of the signal input to the timer input pin (TI), and an interrupt is generated after any delay period.

5.13.2 Simultaneous channel operation function

By using the combination of a master channel (a reference timer mainly controlling the cycle) and slave channels(timers operating according to the master channel), channels can be used for the following purposes.

(1) One-shot pulse output: Two channels are used as a set to generate a one-shot pulse with a specified output timing and a specified pulse width.
(2) PWM (Pulse Width Modulation) output: Two channels are used as a set to generate a pulse with a specified period and a specified duty factor.
(3) Multiple PWM (Pulse Width Modulation) output: Up to 3 PWM signals with arbitrary duty cycles can be generated at a fixed period by expanding the PWM function and using one master channel and multiple slave channels.

5.13.3 8-bit timer operation function

The 8-bit timer operation function makes it possible to use a 16-bit timer channel in a configuration consisting of two 8-bit timer channels. This function can only be used for channels 1 and 3.

5.13.4 LIN-bus supporting function

Timer4 is used to check whether signals received in LIN-bus communication match the LIN-bus communication format.

(1) Detection of wakeup signal: The timer starts counting at the falling edge of a signal input to the serial data input pin (RxD0) of UART0 and the count value of the timer is captured at the rising edge. In this way, a low-level width can be measured. If the low-level width is greater than a specific value, it is recognized as a wakeup signal.
(2) Detection of break field: The timer starts counting at the falling edge of a signal input to the serial data input pin (RxD0) of UART0 after a wakeup signal is detected, and the count value of the timer is captured at the rising edge. In this way,a low-level width is measured. If the low-level width is greater than a specific value, it is recognized as a break field.
(3) Measurement of pulse width of sync field: After a break field is detected, the low-level width and high-level width of the signal input to the serial data input pin (RxD0) of UART0 are measured. From the bit interval of the sync field measured in this way, a baud rate is calculated.

5.14 TimerA

TimerA is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events.

- Timer mode:The count source is counted.
- Pulse output mode:The count source is counted and the output is inverted at each underflow of the timer.
- Event counter mode:An external event is counted. Operation is possible in DEEPSLEEP mode.
- Pulse width measurement mode:An external pulse width is measured.
- Pulse period measurement mode:An external pulse period is measured.

5.15 TimerM

The product contains 2 channels of 16-bit timer timerM optimized for motor control. It has the following 4 working modes:

- Timer mode:
  - Input capture function（Transfer the counter value to a register with an external signal as the trigger）
  - Output compare function（Detect register value matches with a counter,and Pin output can be changed at detection）
  - PWM function（Output pulse of any width continuously）
- Reset synchronous PWM mode:Output three-phase waveforms (6) without sawtooth wave modulation and dead time
- Complementary PWM mode:Output three-phase waveforms (6) with triangular wave modulation and dead time
- PWM3 mode:Output PWM waveforms (2) with a fixed period

5.16 TimerB

TimerB is a 16-bit timer, supports the following three modes:

- Timer mode:
  - Input capture function: Count at the rising edge, falling edge, or both rising/falling edges
  - Output compare function: Low output/high output/toggle output
- PWM mode: PWM output available with any duty cycle
- Phase counting mode: Automatic measurement available for the counts of the two-phase encoder

5.17 TimerC

TimerC is an input capture timer that counts, triggered by a software trigger or comparator 1 and timerM.

5.18 15-bit Interval timer

An interrupt (INTIT) is generated at any previously specified time interval. It can be utilized for wakeup from DEEPSLEEP mode.

5.19 Clock Output/Buzzer Output Controller

The clock output controller is intended for clock output for supply to peripheral ICs. Buzzer output is a function to output a square wave of buzzer frequency.

5.20 Serial communication interface (SCI)

This product has two serial array units. Serial array unit has four serial channels.All channels can achieve UART, simplified SPI (3-wire serial) and simplified I2C.Function assignment of each channel supported by the 64-pin product is as shown below.

5.20.1 3-wire serial I/O（SSPI）

Data is transmitted or received in synchronization with the serial clock (SCK) output from the master channel.3-wire serial communication is clocked communication performed by using three communication lines: one for the serial clock (SCK), one for transmitting serial data (SO), one for receiving serial data (SI).

[Data transmission/reception]

- Data length of 7 or 8 bits
- Phase control of transmit/receive data
- MSB/LSB first selectable

[Clock control]

- Master/slave selection
- Phase control of I/O clock
- Setting of transfer period by prescaler and internal counter of each channel
- Maximum transfer rate

  During master communication: Max. fCLK/2

  During slave communication: Max. fMCK/6

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt

[Error detection flag]

- Overrun error

5.20.2 4-wire serial I/O with Slave Select Input Function

This is a clock synchronization using a slave chip select input (SSI), a serial clock (SCK), a transmit serial data (SO) and a receive serial data (SI) a total of 4 communication lines for communication Communication Interface.

[Data transmission/reception]

- Data length of 7 or 8 bits
- Phase control of transmit/receive data
- MSB/LSB first selectable
- Level setting of transmit/receive data

[Clock control]

- Phase control of I/O clock
- Setting of transfer period by prescaler and internal counter of each channel
- Maximum transfer rate

  During slave communication: Max. fMCK/6

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt

[Error detection flag]

- Overrun error

5.20.3 UART

This is a start-stop synchronization function using two lines: serial data transmission (TxD) and serial data reception(RxD) lines. By using these two communication lines, each data frame, which consist of start bit, data, parity bit,and stop bit, is transferred asynchronously (using the internal baud rate) between the microcontroller and the other communication party. Full-duplex UART communication can be performed by using a channel dedicated to transmission (even-numbered channel) and a channel dedicated to reception (odd-numbered channel). The LIN-bus can be implemented by using UART0, Timer4 unit 0 (channel 3), and an external interrupt (INTP0).

[Data transmission/reception]

- Data length of 7, 8, or 9 bits
- Select the MSB/LSB first
- Level setting of transmit/receive data (selecting whether to reverse the level)
- Parity bit appending and parity check functions
- Stop bit appending, stop bit check function

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt
- Error interrupt in case of framing error, parity error, or overrun error

[Error detection flag]

- Framing error, parity error, or overrun error

[LIN-bus functions]

- Wakeup signal detection
- Break field (BF) detection
- Sync field measurement, baud rate calculation

5.20.4 Simplified I²C

This is a clocked communication function to communicate with two or more devices by using two lines: serial clock (SCL) and serial data (SDA). This simplified I2C is designed for single communication with a device such as EEPROM, flash memory, or A/D converter, and therefore, it functions only as a master.Make sure by using software, as well as operating the control registers, that the AC specifications of the start and stop conditions are observed.

[Data transmission/reception]

- Master transmission, master reception (only for single master application)
- ACK output function and ACK detection function
- Data length of 8 bits (When an address is transmitted, the address is specified by the higher 7 bits, and the least significant bit is used for R/W control.)
- Manual generation of start condition and stop condition

[Interrupt function]

- Transfer end interrupt

[Error detection flag]

- ACK error or overrun error

[Functions not supported by simplified I2C]

- Slave transmission, slave reception
- Arbitration loss detection function
- Wait detection functions

5.21 serial Interface IICA

Serial interface IICA has the following three modes.

- Operation stop mode:
  This mode is used when serial transfers are not performed. It can reduce power consumption.
- I2C bus mode (multi-master application supported):
  This mode is used for 8-bit data transfers with several devices via two lines: a serial clock (SCLAn) line and a serial data bus (SDAAn) line.
  It complies with the I2C bus format and the master device can generated “start condition”, “address”,“transfer direction specification”, “data”, and “stop condition” data to the slave device, via the serial data bus. The slave device automatically detects these received status and data by hardware. It can simplify the part of application program that controls the I2C bus.Since the SCLA and SDAA pins are used for open drain outputs, serial interface IICA requires pull-up resistors for the serial clock line and the serial data bus line.
- Wakeup mode:
  The DEEPSLEEP mode can be released by generating an interrupt request signal (INTIICA) when an extension code from the master device or a local address has been received while in DEEPSLEEP mode.

5.22 Controller CAN

This product supports CAN bus interface.

- Comply with ISO 11898 and test according to ISO/DIS 16845 (CAN compliance)
- Use standard frame and extended frame to realize reception and transmission
- Communication speed: maximum 1 Mbps (CAN input clock 8 MHz)
- 1 channel has 16 message buffers
- Receive/send history list function
- Automatic block transmission function
- Multi-cache receiving block function
- Four modes of shielding setting for each channel

5.23 A/D Converter（ADC）

The A/D converter is a converter that converts analog input signals into digital values, and is configured to control analog inputs, including up to 17 channels of A/D converter analog inputs (ANI0 to ANI15).

The A/D converter has the following function.

- 12-bit resolution A/D conversion, Conversionrate 1.06Msps.
- Trigger mode:Software trigger, Hardware trigger mode
- Channel selection:Sigle channel select mode and Scan mode
- Conversion operation mode:One-shot conversion mode and Sequential conversion mode
- Operation voltage:2.0V≤VDD≤5.5V
- Can detect the internal reference voltage (1.45V) and temperature sensor.

Various A/D conversion modes can be specified by using the mode combinations below.

Trigger mode	Software trigger	Conversion is started by software.
	Hardware trigger no-wait mode	Conversion is started by detecting a hardware trigger.
	Hardware trigger wait mode	The power is turned on by detecting a hardware trigger while the system is off and in the conversion standby state, and conversion is then started automatically after the stabilization wait time passes.
Channel selection mode	Select mode	A/D conversion is performed on the analog input of one selected channel.
	Scan mode	A/D conversion is performed on the analog input of four channels in order. Fou consecutive channels can be selected from ANI0 to ANI15 as analog input channels.
Conversion operation mode	One-shot conversion mode	A/D conversion is performed on the selected channel once.
	Sequential conversion mode	A/D conversion is sequentially performed on the selected channels until it is stopped by software.
Sampling time/ Conversion time	Sampling clock cycles / Conversion clock cycles	The sampling time can be set by the register. The default value of the sampling clock is 13.5 clk, and the conversion clock number Min is 31.5 clk.

5.24 D/A converter（DAC）

The D/A converter is an 8-bit resolution converter that converts digital inputs into analog signals. It is used to control analog outputs for two independent channels.The D/A converter has the following features.:

- 8-bit resolution
- 2 channels
- R-2R ladder method
- Real-time output

5.25 programmable gain amplifier（PGA）

This product has two programmable gain amplifiers（PGA0,PGA1）, The programmable gain amplifier is provided with the following functions.

- GAIN: X4, X8, X10, X12, X14, X16, X32
- The external pin(PGAGND) can be selected as the ground of the negative feedback resistance of the PGA
- The output of PGA0 can be selected as the analog input for the A/D converter or the analog input of the positive terminal of comparator 0 (CMP0)
- PGA1 output can be selected as analog input for A/D converter

5.26 comparator（CMP）

The product has two comparator channels, The comparator has the following functions.

- A pin selector switch is added to the analog input of CMP1.
- The external reference voltage input or internal reference voltage can be selected as the reference voltage.
- The canceling width of the noise canceling digital filter can be selected.
- An interrupt signal can be generated by detecting an active edge of the comparator output.
- An event link controller (EVENTC) event signal can be output by detecting an active edge of the comparator output.

5.27 Serial wire debug（SW-DP）

SW-DP interface allows connection to the microcontroller via serial line debugging tools.

5.28 Safety Functions

5.28.1 Flash memory CRC operation function (high-speed CRC, general-purpose CRC)

This detects data errors in the flash memory by performing CRC operations.
Two CRC functions are provided according to the different applications.

- High-speed CRC:The CPU can be stopped and a high-speed check executed on its entire code flash memory area during the initialization routine.
- General CRC:This can be used for checking various data in addition to the code flash memory area while the CPU is running.

5.28.2 RAM parity error detection function

This detects parity errors when the RAM is read as data.

5.28.3 SFR guard function

This prevents SFRs（Special Function Register）from being rewritten when the CPU freezes.

5.28.4 Invalid memory access detection function

This detects illegal accesses to invalid memory areas.

5.28.5 Frequency detection function

This uses the timer4 to perform a self-check of the CPU/peripheral hardware clock frequency.

5.28.6 A/D test function

This is used to perform a self-check of A/D converter by performing A/D conversion on the positive internal reference voltage, negative reference voltage, analog input channel (ANI), temperature sensor output, and internal reference voltage output.

5.28.7 Digital output signal level detection function

When the I/O pins are output mode, the output level of the pin can be read.

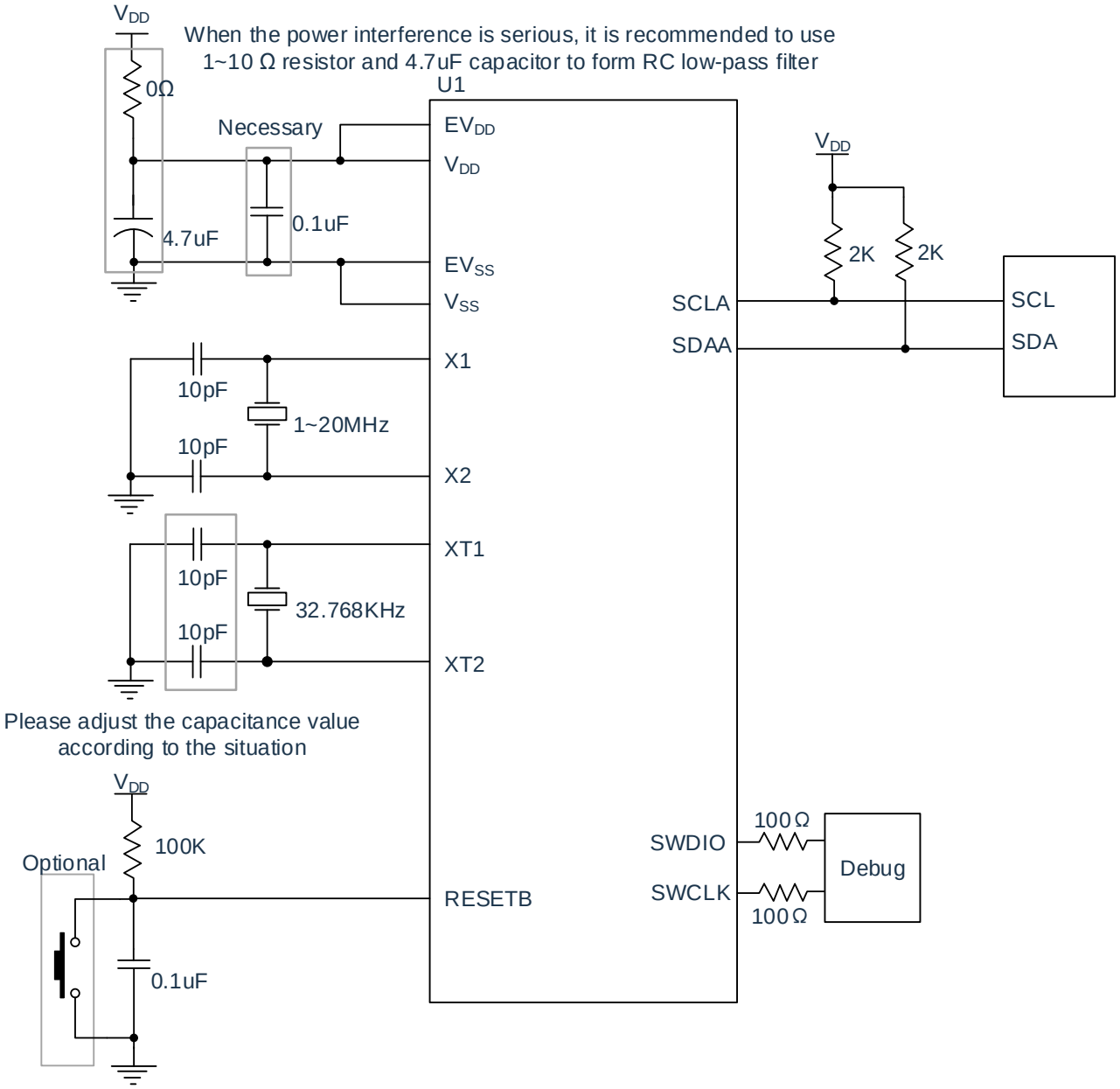
5.29 Key Function

A key interrupt (INTKR) can be generated by inputting a falling edge to the key interrupt input pins (KR0 to KR7).

6 Electrical Characteristics

6.1 Typical application peripheral circuit

The connection reference of the MCU typical application peripheral circuit is as follows:



6.2 Absolute maximum voltage ratings

（TA=–40～+105℃）

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	VDD		–0.5～+6.5	V
	EVDD		–0.5～+6.5	V
Input voltage	VI1	P00～P06, P10～P17, P30, P31, P40～P43, P50～P55, P70～P77, P120, P136, P140, P141, P146, P147	–0.3～EVDD+0.3 and –0.3～VDD+0.3 note1	V
	VI2	P60～P63(N-ch open-drain）	–0.3～+6.5	V
	VI3	P20～P27, P121～P124, P137, EXCLK, EXCLKS, RESETB	–0.3～VDD+0.3 note1	V
Output voltage	VO1	P00～P06, P10～P17, P30, P31, P40～P43, P50～P55, P60～P63, P70～P77, P120, P130, P136, P140, P141, P146, P147	–0.3～EVDD+0.3 and –0.3～VDD+0.3 note1	V
	VO2	P20～P27, P137	–0.3～VDD+0.3 note1	V
Analog input voltage	VAI1	ANI8～ANI12	–0.3～EVDD+0.3 and –0.3～AVREF(+)+0.3 note1, 2	V
	VAI2	ANI0～ANI7	–0.3～VDD+0.3 and –0.3～AVREF(+)+0.3 note1, 2	V

note:

1. Must be 6.5 V or lower.
2. Do not exceed AVREF (+) + 0.3 V in case of A/D conversion target pin.

Caution:

Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter.

That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark:

1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
2. AVREF (+): + side reference voltage of the A/D converter.
3. VSS: Reference voltage

6.3 Absolute maximum current ratings

（TA=–40～+105℃）

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	IOH1	Per pin	P00～P06, P10～P17, P30, P31, P40～P43, P50～P55, P70～P77, P120, P130, P136, P137, P140, P141, P146, P147	–40	mA
		Total of all pins –170mA	P00～P04, P40～P43, P120, P130, P136, P137, P140, P141	–70	mA
			P05, P06, P10～P17, P30, P31, P50～P55, P70～P77, P146, P147	–100	mA
	IOH2	Per pin	P20～P27	–3	mA
		Total of all pins		–15	mA
Output current, low	IOL1	Per pin	P00～P06, P10～P17, P30, P31, P40～P43, P50～P55, P60～P63, P70～P77, P120, P130, P136, P137, P140, P141, P146, P147	40	mA
		Total of all pins 170mA	P00～P04, P40～P43, P120, P130, P136, P137, P140, P141	100	mA
			P05, P06, P10～P17, P30, P31, P50～P55, P70～P77, P146, P147	120	mA
	IOL2	Per pin	P20～P27	15	mA
		Total of all pins		45	mA
Input negative current	I_{INJL}	Each pin	Continuous DC negative current that can be injected into an input pin	-3	mA
		Pin total		-15	mA
Input positive current	I_{INJH}	Each pin	Continuous DC positive current that can be injected into an input pin	3	mA
		Pin total		15	mA
Operating ambient temperature	TA	In normal operation mode		–40～+105	℃
		In flash memory programming mode			
Storage temperature	Tstg	-		–65～+150	℃

Caution:

Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter.

That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark: Unless otherwise specified, the characteristics of the multiplexed pin are the same as the characteristics of the port pin.

6.4 Oscillator Characteristics

6.4.1 X1, XT1 characteristics

（TA=–40～+105℃, 2.0V≤VDD≤5.5V, VSS=0V）

Resonator	Resonator	Conditions	MIN	TYP	MAX	Unit
X1 clock oscillation frequency (fx)	Ceramic resonator/		1.0	-	20.0	MHz
X1 clock oscillation satable time	crystal resonator	20MHz，C=10pF		15		mS
X1 clock oscillation Transconductance(gm)	crystal resonator	AMPH=0	0.4	1.2	2.2	mA/V
	crystal resonator	AMPH=1	0.7	1.8	2.3	mA/V
X1 clock oscillation Feedback resistance	Ceramic resonator/		0.6		1.8	MΩ
XT1 clock oscillation frequency (fxt)	Crystal resonator		32	32.768	35	kHz
XT1 clock oscillation satable time	Crystal resonator	32.768kHz，C=10pF		2		S

Remark:

1. It only indicates the frequency tolerance range of the oscillation circuit, and the command execution time should refer to the AC characteristics.
2. Please entrust the resonator manufacturer with an evaluation after installing the circuit and use it after checking the oscillation characteristics.

6.4.2 On-chip oscillator characteristics

（TA=–40～+105℃, 2.0V≤VDD≤5.5V, VSS=0V）

Oscillators	Conditions	MIN	TYP	MAX	Unit
High-speed on-chip oscillator clock frequency (fIH) 注1,2	-	1.0		64.0	MHz
High-speed on-chip oscillator satable time (tSU)	-		12		uS
High-speed on-chip oscillator clock frequency accuracy	TA= + 10～ +70℃	-1.0		+1.0	%
	TA=–10～ +105℃	-1.5 注3		+1.5 注3	%
	TA=–20～ +105℃	-2.0 注3		+2.0 注3	%
	TA=–40～ +105℃	-4.0 注3		+4.0 注3	%
Low-speed on-chip oscillator clock frequency (fIL)	-	10	15	20	kHz

Note:

1. High-speed on-chip oscillator frequency is selected with the option byte and HOCODIV register.
2. This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.
3. The low temperature specification value is guaranteed by the design, and the low temperature condition is not tested in mass production.

6.5 DC Characteristics

6.5.1 Pin Characteristics

（TA=–40～+105℃, 2.0V≤EVDD=VDD≤5.5V, VSS=Evss=0V）

Items	Symbol	Conditions		MIN	TYP	MAX	Unit
Output current, high Note 1	IOH1	P00～P06、P10～P17、P30、P31、P40～P43、P50～P55、P70～P77、P120、P130、P136、P137、P140、P141、P146、P147 Per pin	2.0V≤EVDD≤5.5V –40～+85℃			-12.0 注2	mA
			2.0V≤EVDD≤5.5V 85～+105℃			-6.0 注2	
		P00～P04、P40～P43、P120、P130、P136、P137、P140、P141 Total of all pins (When duty ≤ 70% Note 3)	4.0V≤EVDD≤5.5V –40～+85℃			-60.0	mA
			4.0V≤EVDD≤5.5V 85～+105℃			-30.0	
			2.4V≤EVDD＜4.0V			-12.0	mA
			2.0V≤EVDD＜2.4V			-6.0	mA
		P05、P06、P10～P17、P30、P31、P50～P53、P70～P77、P146、P147 Total of all pins (When duty ≤ 70% Note 3)	4.0V≤EVDD≤5.5V –40～+85℃			-80.0	mA
			4.0V≤EVDD≤5.5V 85～+105℃			-30.0	
			2.4V≤EVDD＜4.0V			-20.0	mA
			2.0V≤EVDD＜2.4V			-10.0	mA
		Total of all pins (When duty ≤ 70% Note 3)	2.0V≤EVDD≤5.5V –40～+85℃			-140.0	mA
			2.0V≤EVDD≤5.5V 85～+105℃			-60.0	
	IOH2	Per pin for P20 ～ P27	2.0V≤VDD≤5.5V			-2.5 注2	mA
		Total of all pins (When duty ≤ 70% Note 3)	2.0V≤VDD≤5.5V			-10	mA

Note:

1. Value of current at which the device operation is guaranteed even if the current flows from the EVDD, VDD pins to an output pin.
2. Do not exceed the total current value.
3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor ＞ 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

• Total output current of pins = (IOH × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOH = -10.0 mA

Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Note: In N-channel open-drain mode, P00, P02~P04, P10, P11, P13~P15, P17, P30, P50, P51, P55, P71, The P74 does not output a high level (for example, a 64-pin product).

Remark: Unless otherwise specified, the characteristics of the multiplexed pin are the same as the characteristics of the port pin.

（TA=–40～+105℃, 2.0V≤EVDD=VDD≤5.5V, VSS=Evss=0V）

Items	Symbol	Conditions		MIN	TYP	MAX	Unit
Output current, low Note 1	IOL1	Per pin for P00～P06, P10～P17, P30, P31, P40～P43, P50～P55, P60～P63, P70～P77, P120, P130, P136, P137, P140, P141, P146, P147	2.0V≤EVDD≤5.5V –40～+85℃			35Note2	mA
			2.0V≤EVDD≤5.5V 85～+105℃			20Note2	
		Total of P00～P04, P40～P43, P120, P130, P136, P137, P140, P141 (When duty ≤ 70% Note 3)	4.0V≤EVDD≤5.5V –40～+85℃			100	mA
			4.0V≤EVDD≤5.5V 85～+105℃			70	
			2.4V≤EVDD＜4.0V			30	mA
			2.0V≤EVDD＜2.4V			15	mA
		Total of P05, P06, P10～P17, P30, P31, P50～P55, P60～P63, P70～P77, P146, P147 (When duty ≤ 70% Note 3)	4.0V≤EVDD≤5.5V –40～+85℃			120	mA
			4.0V≤EVDD≤5.5V 85～+105℃			80	
			2.4V≤EVDD＜4.0V			40	mA
			2.0V≤EVDD＜2.4V			20	mA
		Total of all pins (When duty ≤ 70% Note 3)	2.0V≤EVDD≤5.5V –40～+85℃			150	mA
			2.0V≤EVDD≤5.5V 85～+105℃			100	
	IOL2	Per pin for P20～P27	2.0V≤VDD≤5.5V			10Note2	mA
		Total of all pins (When duty ≤ 70% Note 3)	2.0V≤VDD≤5.5V			40	mA

Note:

1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EVSS0 and VSS pins.
2. Do not exceed the total current value.
3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor ＞ 70% the duty ratio can be calculated with the following

expression (when changing the duty factor from 70% to n%).

• Total output current of pins = (IOL × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOL = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Remark: Unless otherwise specified, the characteristics of the multiplexed pin are the same as the characteristics of the port pin.

（TA=–40～+105℃, 2.0V≤EVDD=VDD≤5.5V, VSS=Evss=0V）

Items	Symbol	Conditions		MIN	TYP	MAX	Unit
Power input voltage	VDD EVDD	-		2.0		5.5	
Power ground input voltage	VSS EVSS	-		-0.3			
Input voltage, high	VIH1	P00～P06, P10～P17, P30, P31, P40～P43, P50～P55, P70～P77, P120, P136, P140, P141, P146, P147	Schmitt input	0.8EVDD		EVDD	V
	VIH2	P01, P03, P04, P10, P14～P17, P30, P50, P55	TTL input 4.0V≤EVDD≤5.5V	2.2		EVDD	V
			TTL input 3.3V≤EVDD＜4.0V	2.0		EVDD	V
			TTL input 2.0V≤EVDD＜3.3V	1.5		EVDD	V
	VIH3	P20～P27, P137		0.7VDD		VDD	V
	VIH4	P60～P63		0.7EVDD		6.0	V
	VIH5	P121～P124, EXCLK, EXCLKS, RESETB		0.8VDD		VDD	V
Input voltage, low	VIL1	P00～P06, P10～P17, P30, P31, P40～P43, P50～P55, P70～P77, P120, P136, P140, P141, P146, P147	Schmitt input	0		0.2EVDD	V
	VIL2	P01, P03, P04, P10, P14～P17, P30, P50, P55	TTL input 4.0V≤EVDD≤5.5V	0		0.8	V
			TTL input 3.3V≤EVDD＜4.0V	0		0.5	V
			TTL input 2.0V≤EVDD＜3.3V	0		0.32	V
	VIL3	P20～P27, P137		0		0.3VDD	V
	VIL4	P60～P63		0		0.3EVDD	V
	VIL5	P121～P124, EXCLK, EXCLKS, RESETB		0		0.2VDD	V

Caution:

The maximum value of VIH of pins P00, P02～P04, P10, P11, P13～P15, P17, P30, P50, P51, P55, P71, P74 is EVDD, even in the N-ch open-drain mode.（64-pin products as an example）.

Remark: Unless otherwise specified, the characteristics of the multiplexed pin are the same as the characteristics of the port pin.

（TA=–40 ～ +105℃, 2.0V≤EVDD=VDD≤5.5V, VSS=Evss=0V）

Items	Symbol	Conditions		MIN	TYP	MAX	Unit
Output voltage, high	VOH1	P00～P06, P10～P17, P30, P31, P40～P43, P50～P55, P70～P77, P120, P130, P136, P137, P140, P141, P146, P147	4.0V≤EVDD≤5.5V, IOH1=–12.0mA	EVDD–1.5			V
			4.0V≤EVDD≤5.5V, IOH1=–6.0mA	EVDD–0.7			V
			2.4V≤EVDD≤5.5V, IOH1=–3.0mA	EVDD–0.6			V
			2.0V≤EVDD≤5.5V, IOH1=–2mA	EVDD–0.5			V
	VOH2	P20～P27	4.0V≤VDD≤5.5V, IOH2=–2.5mA	EVDD–1.5			V
			4.0V≤VDD≤5.5V, IOH2=–1.5mA	EVDD–0.7			V
			2.4V≤VDD≤5.5V, IOH2=–0.5mA	EVDD–0.6			V
			2.0V≤VDD≤5.5V, IOH2=–0.4mA	VDD–0.5			V
Output voltage, low	VOL1	P00～P06, P10～P17, P30, P31, P40～P43, P50～P55, P60～P63, P70～P77, P120, P130, P136, P137, P140, P141, P146, P147	4.0V≤EVDD≤5.5V, IOL1=35.0mA			1.2	V
			4.0V≤EVDD≤5.5V, IOL1=20.0mA			0.7	V
			2.4V≤EVDD≤5.5V, IOL1=9.0mA			0.4	V
			2.0V≤EVDD≤5.5V, IOL1=7.0mA			0.4	V
	VOL2	P20～P27	4.0V≤VDD≤5.5V, IOL2=10.0mA			1.2	V
			4.0V≤VDD≤5.5V, IOL2=6.0mA			0.7	V
			2.4V≤VDD≤5.5V, IOL2=2.5mA			0.4	V
			2.0V≤VDD≤5.5V, IOL2=2.0mA			0.4	V

Caution:

The maximum value of VIH of pins P00, P02～P04, P10, P11, P13～P15, P17, P30, P50, P51, P55, P71, P74 is EVDD, even in the N-ch open-drain mode.（64-pin products as an example）.

Remark: Unless otherwise specified, the characteristics of the multiplexed pin are the same as the characteristics of the port pin.

（TA=–40～+105℃, 2.0V≤EVDD=VDD≤5.5V, VSS=Evss=0V）

Items	Symbol	Conditions		MIN	TYP	MAX	Unit
Input leakage current, high	ILIH1	P00～P06, P10～P17, P30, P31, P40～P43, P50～P55, P70～P77, P120, P136, P140, P141, P146, P147	VI=EVDD			1	μA
	ILIH2	P20～P27, P137, RESETB	VI=VDD			1	μA
	ILIH3	P121～P124 （X1, X2, EXCLK, XT1, XT2, EXCLKS）	VI=VDD, In input port or external clock input			1	μA
			VI=VDD, In resonator connection			10	μA
Input leakage current, low	ILIL1	P00～P06, P10～P17, P30, P31, P40～P43, P50～P55, P70～P77, P120, P136, P140, P141, P146, P147	VI=EVSS			-1	μA
	ILIL2	P20～P27, P137, RESETB	VI=VSS			-1	μA
	ILIL3	P121～P124 （X1, X2, EXCLK, XT1, XT2, EXCLKS）	VI=VSS, In input port or external clock input			-1	μA
			VI=VSS, In resonator connection			-10	μA
On-chip pull-up resistance	RU	P00～P06, P10～P17, P30, P31, P40～P43, P50～P55, P70～P77, P120, P136, P137, P140, P141, P146, P147	VI=EVSS, In input port	10	30	100	kΩ

Remark: Unless otherwise specified, the characteristics of the multiplexed pin are the same as the characteristics of the port pin.

6.5.2 Supply current characteristics

（TA=–40～+105℃, 2.0V≤EVDD=VDD≤5.5V, VSS=EVSS=0V）

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	High-speed on-chip oscillator	f_{HOCO}=64MHz, f_{IH}=32MHz note3			3.9	7.1	mA
				f_{HOCO}=48MHz, f_{IH}=48MHz note3			4.0	7.9	
				f_{HOCO}=32MHz, f_{IH}=32MHz note3			3.6	6.6	
			high-speed main clock	f_{MX}=20MHz note2	Square wave		2.3	4.3	mA
					Resonator		2.3	4.3	
			high-speed SUB clock	f_{SUB}=32.768kHz note 4	Square wave		70	85	uA
					Resonator		70	85	
	I_{DD2}	Sleep mode	High-speed on-chip oscillator	f_{HOCO}=64MHz, f_{IH}=32MHz note3			1.2	3.2	mA
				f_{HOCO}=48MHz, f_{IH}=48MHz note3			1.2	3.7	
				f_{HOCO}=32MHz, f_{IH}=32MHz note3			1.2	2.6	
			high-speed main clock	f_{MX}=20MHz note2	Square wave		0.7	1.8	mA
					Resonator		0.7	1.8	
			high-speed SUB clock	f_{SUB}=32.768kHz note5	Square wave		0.7	13	uA
					Resonator		0.7	13	
	I_{DD3} note6	Deep Sleep mode note 7	T_A=–40℃~+70℃ VDD=3.0V				0.45	3.0	uA
			T_A=–40℃~+85℃ VDD=3.0V				0.45	5.0	
			T_A=–40℃~+105℃ VDD=3.0V				0.45	12.5	

Note:

1. Total current flowing into VDD and EVDD, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDD or VSS, EVSS. The values of the TYP. column include the current of the CPU executing the multiplication instruction (IDD1),not including the peripheral operation current. The values below the MAX. column include the current of the CPU executing the multiplication instruction (IDD1) and the peripheral operation current.However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
2. When high-speed on-chip oscillator and subsystem clock are stopped.
3. When high-speed system clock and subsystem clock are stopped.
4. When high-speed on-chip oscillator and high-speed system clock are stopped.
5. When high-speed on-chip oscillator and high-speed system clock are stopped. The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
7. Regarding the value for current to operate the subsystem clock in DeepSleep mode, refer to that in Sleep mode.

Remark:

1. fHOCO :High-speed on-chip oscillator clock frequency. fIH :High-speed on-chip oscillator systerm clock frequency.
2. fSUB :Subsystem clock frequency (XT1/XT2 clock oscillation frequency).
3. fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency).
4. temperature condition of the TYP. value is TA = 25℃.

（TA=–40～+105℃, 2.0V≤EVDD=VDD≤5.5V, VSS=EVSS=0V）

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	IFIL note1				0.2		uA
RTC operating current	IRTC note1,2,3				0.04		uA
15-bit interval timer operating current	IIT note1,2,4				0.02		uA
Watchdog timer operating current	IWDT note1,2,5	fIL=15kHz			0.22		uA
A/D operating current	IADC note1,6	ADC HS mode@64MHz			2.2		mA
		ADC HS mode @4MHz			1.3		mA
		ADC LC mode @24MHz			1.1		mA
		ADC LC mode @4MHz			0.8		mA
D/A operating current	IDAC note1,8	Per D/A converter channel			1.4		mA
PGA operating current		Per PGA channel			480	700	uA
CMP operating current	ICMP note1,9	Per CMP channel	When the internal reference voltage is not in use		60	100	uA
			When the internal reference voltage is in use		80	140	uA
LVD operating current	ILVD note1,7				0.08		uA

Note:

1. Current flowing to VDD.
2. When high speed on-chip oscillator and high-speed system clock are stopped.
3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the microcontrollers is the sum of the values of either IDD1 or IDD2, and IRTC, when the real-time clock operates in operation mode or Sleep mode. When the low-speed on-chip oscillator is selected, IFIL should be added. IDD2 subsystem clock operation includes the operational current of the real-time clock.
4. Current flowing only to the 15-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the microcontrollers is the sum of the values of either IDD1 or IDD2, and IIT, when the 15-bit interval timer operates in operation mode or Sleep mode. When the low-speed on-chip oscillator is selected, IFIL should be added.
5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator).
6. Current flowing only to the A/D converter. The supply current of the microcontrollers is the sum of IDD1 or IDD2 and IADC when the A/D converter operates in an operation mode or the Sleep mode.
7. Current flowing only to the LVD circuit. The supply current of the microcontrollers is the sum of IDD1, IDD2 or IDD3 and ILVD when the LVD circuit is in operation.
8. Current flowing only to the D/A converter. The supply current of the microcontrollers is the sum of IDD1 or IDD2 and IDAC when the D/A converter operates in an operation mode or the Sleep mode.

9. Current flowing only to the comparator circuit. The supply current of the microcontrollers is the sum of IDD1, IDD2, or IDD3 and ICMP when the comparator circuit is in operation.

Remark:

1. fIL :Low-speed on-chip oscillator clock frequency
2. temperature condition of the TYP. value is TA = 25℃.

6.6 AC Characteristics

（TA=–40～+105℃, 2.0V≤EVDD=VDD≤5.5V, VSS=EVSS=0V）

Items	Symbol	Conditions		MIN	TYP	MAX	Unit
Instruction cycle (minimum instruction execution time)	TCY	Main system clock (fMAIN)operation	2.0V≤VDD≤5.5V	0.02084		1	μs
		Subsystem clock (fSUB) operation	2.0V≤VDD≤5.5V	28.5	30.5	31.3	μs
External system clock frequency	fEX	2.0V≤VDD≤5.5V		1.0		20.0	MHz
	fEXS	2.0V≤VDD≤5.5V		32.0		35.0	kHz
External system clock input high-level width, low-level width	tEXH, tEXL	2.0V≤VDD≤5.5V		24			ns
	tEXHS, tEXLS	2.0V≤VDD≤5.5V		13.7			μs
TI00 ～ TI03, input high-level width, low-level width	tTIH, tTIL	2.0V≤VDD≤5.5V		1/fMCK+10			ns
timerA input cycle	tC	TAIO	2.4V≤EVDD≤5.5V	100			ns
			2.0V≤EVDD＜2.4V	300			ns
timerA input highlevel width, low-level width	tTAIH, tTAIL	TAIO	2.4V≤EVDD≤5.5V	40			ns
			2.0V≤EVDD＜2.4V	120			ns

Remark: F_{MCK}: The operating clock frequency of the Timer4 unit

（TA=–40～+105℃, 2.0V≤EVDD=VDD≤5.5V, VSS=EVSS =0V）

Items	Symbol	Conditions		MIN	TYP	MAX	Unit
TimerM input high-level width, low-level width	tTMIH, tTMIL	TMIOA0, TMIOA1, TMIOB0, TMIOB1, TMIOC0, TMIOC1, TMIOD0, TMIOD1		3/fCLK			ns
TimerM forced cutoff signal input low-level width	tTMSIL	P136/INTP0	2MHz＜ fCLK≤48MHz	1			μs
			fCLK ≤ 2MHz	1/fCLK+1			μs
TimerB input high-level width, low-level width	tTBIH, tTBIL	TBIOA, TBIOB		2.5/fCLK			ns
TO00 ～ TO03, TAIO0, TAO0, TMIOA0, TMIOA1, TMIOB0, TMIOB1, TMIOC0, TMIOC1, TMIOD0, TMIOD1, TBIOA, TBIOB output frequency	fTO	4.0V≤EVDD≤5.5V				16	MHz
		2.4V≤EVDD＜4.0V				8	MHz
		2.0V≤EVDD＜2.4V				4	MHz
CLKBUZ0, CLKBUZ1 output frequency	fPCL	4.0V≤EVDD≤5.5V				16	MHz
		2.4V≤EVDD＜4.0V				8	MHz
		2.0V≤EVDD＜2.4V				4	MHz
Interrupt input high-level width, low-level width	tINTH, tINTL	INTP0 ～ INTP11	2.0V≤EVDD≤5.5V	1			μs
Key interrupt input low-level width	tKR	KR0 ～ KR7	2.0V≤EVDD≤5.5V	250			ns
RESETB low-level width	tRSL			10			μs

6.7 Peripheral Functions Characteristics

6.7.1 Serial communication interface

1) UART mode

・（TA=–40～+85℃, 2.0V≤EVDD=VDD≤5.5V, VSS=EVSS=0V）

Parameter	Conditions		Spec		Unit
			MIN	MAX	
Transfer rate	2.0V ≤ EVDD ≤ 5.5V			fMCK/6	bps
		Theoretical value of the maximum transfer rate fMCK=fCLK		8	Mbps

・（TA=+85～+105℃, 2.0V≤EVDD=VDD≤5.5V, VSS=EVSS=0V）

Parameter	Conditions				Unit
			MIN	MAX	
Transfer rate	2.0V ≤ EVDD ≤ 5.5V			fMCK/12	bps
		Theoretical value of the maximum transfer rate fMCK=fCLK		4	Mbps

2) 3-wire serial I/O（SSPI）（master mode, internal clock output）

（TA=–40～+105℃, 2.0V≤EVDD=VDD≤5.5V, VSS=EVSS=0V）

Parameter	Symbol	Conditions		–40 ～ +85℃		+85 ～ +105℃		Unit
				MIN	MAX	MIN	MAX	
SCLKp cycle time	tKCY1	tKCY1 ≥ 2/fCLK	4.0V ≤ EVDD ≤ 5.5V	41.67		83.33		ns
			2.7V ≤ EVDD ≤ 5.5V	83.33		166.67		
			2.4V ≤ EVDD ≤ 5.5V	125		250		ns
			2.0V ≤ EVDD ≤ 5.5V	250		500		ns
SCLKp high-/low-level width	tKH1, tKL1	4.0V ≤ EVDD ≤ 5.5V		tKCY1/2–7		tKCY1/2–14		ns
		2.7V ≤ EVDD ≤ 5.5V		tKCY1/2–10		tKCY1/2–20		ns
		2.4V ≤ EVDD ≤ 5.5V		tKCY1/2–18		tKCY1/2–36		ns
		2.0V ≤ EVDD ≤ 5.5V		tKCY1/2–38		tKCY1/2–76		ns
SDIp setup time (to SCLKp↑)	tSIK1	4.0V ≤ EVDD ≤ 5.5V		23		46		ns
		2.7V ≤ EVDD ≤ 5.5V		33		66		ns
		2.4V ≤ EVDD ≤ 5.5V		44		88		ns
		2.0V ≤ EVDD ≤ 5.5V		75		113		ns
SDIp hold time (from SCLKp↑)	tKSI1	2.0V ≤ EVDD ≤ 5.5V		10		20		ns
SCLKp↓→ SDOp Delay time	tKSO1	2.0V ≤ EVDD ≤ 5.5V C=20pF Note1			10		20	ns

Note 1. C is the load capacitance of the SCLKp and SDOp output lines.

Caution: Select the normal input buffer for the SDIp pin and the normal output mode for the SDOp pin and SCLKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

3) 3-wire serial I/O（SSPI）（slave mode, external clock input）

（TA=–40～+105℃, 2.0V≤EVDD=VDD≤5.5V, VSS=EVSS=0V）

Parameter	Symbol	Conditions		–40 ～ +85℃		+85 ～ +105℃		Unit
				MIN	MAX	MIN	MAX	
SCLKp cycle time	tKCY2	4.0V ≤ EVDD ≤ 5.5V	20MHz < fMCK	8/fMCK		16/fMCK		ns
			fMCK ≤20MHz	6/fMCK		12/fMCK		ns
		2.7V ≤ EVDD ≤ 5.5V	16MHz < fMCK	8/fMCK		16/fMCK		ns
			fMCK ≤16MHz	6/fMCK		12/fMCK		ns
		2.4V ≤ EVDD ≤ 5.5V		6/fMCK and 500		12/fMCK and 1000		ns
		2.0V ≤ EVDD ≤ 5.5V		6/fMCK and 750		12/fMCK and 1500		ns
SCLKp high-/low-level width	tKH2, tKL2	4.0V ≤ EVDD ≤ 5.5V		tKCY1/2–7		tKCY1/2–14		ns
		2.7V ≤ EVDD ≤ 5.5V		tKCY1/2–8		tKCY1/2–16		ns
		2.0V ≤ EVDD ≤ 5.5V		tKCY1/2–18		tKCY1/2–36		ns
SDIp setup time (to SCLKp↑)	tSIK2	2.7V ≤ EVDD ≤ 5.5V		1/fMCK+20		1/fMCK+40		ns
		2.0V ≤ EVDD ≤ 5.5V		1/fMCK+30		1/fMCK+60		ns
SDIp hold time (from SCLKp↑)	tKSI2	2.0V ≤ EVDD ≤ 5.5V		1/fMCK+31		1/fMCK+62		ns
SCLKp↓→ SDOp Delay time	tKSO2	2.7V ≤ EVDD ≤ 5.5V C=30pF note1			2/fMCK +44		2/fMCK +66	ns
		2.4V ≤ EVDD ≤ 5.5V C=30pF note1			2/fMCK +75		2/fMCK +113	ns
		2.0V ≤ EVDD ≤ 5.5V C=30pF note1			2/fMCK +100		2/fMCK +150	ns

Note 1. C is the load capacitance of the SCLKp and SDOp output lines.

Caution: Select the normal input buffer for the SDIp pin and the normal output mode for the SDOp pin and SCLKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

4) 4-wire serial I/O（SPI）（slave mode, external clock input）

（TA=–40～+105℃, 2.0V≤EVDD=VDD≤5.5V, VSS=EVSS=0V）

Parameter	Symbol	Conditions		–40 ～ +85℃		+85 ～ +105℃		Unit
				MIN	MAX	MIN	MAX	
SSI00 setup time	tSSIK	DAPmn=0	2.7V ≤ EVDD ≤ 5.5V	120		240		ns
			2.0V ≤ EVDD ≤ 5.5V	200		400		ns
		DAPmn=1	2.7V ≤ EVDD ≤ 5.5V	1/fMCK+120		1/fMCK+240		ns
			2.0V ≤ EVDD ≤ 5.5V	1/fMCK+200		1/fMCK+400		ns
SSI00 hold time	tKSSI	DAPmn=0	2.7V ≤ EVDD ≤ 5.5V	1/fMCK+120		1/fMCK+240		ns
			2.0V ≤ EVDD ≤ 5.5V	1/fMCK+200		1/fMCK+400		ns
		DAPmn=1	2.7V ≤ EVDD ≤ 5.5V	120		240		ns
			2.0V ≤ EVDD ≤ 5.5V	200		400		ns

Caution: Select the normal input buffer for the SDIp pin and the normal output mode for the SDOp pin and SCLKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

5) simplified I²C mode

（TA=–40～+105℃, 2.0V≤EVDD=VDD≤5.5V, VSS=EVSS=0V）

Parameter	Symbol	Conditions	–40 ～ +85℃		+85 ～ +105℃		Unit
			MIN	MAX	MIN	MAX	
SCLr clock frequency	fSCL	2.7V ≤ EVDD ≤ 5.5V C_b = 50 pF, R_b = 2.7 kΩ		1000note1		400Note1	kHz
		2.0V ≤ EVDD ≤ 5.5V C_b = 100 pF, R_b = 3 kΩ		400note1		100Note1	kHz
		2.0V ≤ EVDD ≤ 2.7V C_b = 100 pF, R_b = 5 kΩ		300note1		75Note1	kHz
Hold time when SCLr = “L”	t_{LOW}	2.7V ≤ EVDD ≤ 5.5V C_b = 50 pF, R_b = 2.7 kΩ	475		1200		ns
		2.0V ≤ EVDD ≤ 2.7V C_b = 100 pF, R_b = 3 kΩ	1150		4600		ns
		2.0V ≤ EVDD ≤ 2.7V C_b = 100 pF, R_b = 5 kΩ	1550		6500		ns
Hold time when SCLr = “H”	t_{HIGH}	2.7V ≤ EVDD ≤ 5.5V Cb = 50 pF, Rb = 2.7 kΩ	475		1200		ns
		2.0V ≤ EVDD ≤ 2.7V Cb = 100 pF, Rb = 3 kΩ	1150		4600		ns
		2.0V ≤ EVDD ≤ 2.7V Cb = 100 pF, Rb = 5 kΩ	1550		6500		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7V ≤ EVDD ≤ 5.5V Cb = 50 pF, Rb = 2.7 kΩ	1/fMCK+85 note2		1/fMCK+ 220note2		ns
		2.0V ≤ EVDD ≤ 5.5V Cb = 100 pF, Rb = 3 kΩ	1/fMCK+145 note2		1/fMCK+ 580note2		ns
		2.0V ≤ EVDD ≤ 2.7V Cb = 100 pF, Rb = 5 kΩ	1/fMCK+230 note2		1/fMCK+ 1200note2		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7V ≤ EVDD ≤ 5.5V Cb = 50 pF, Rb = 2.7 kΩ		305		770	ns
		2.0V ≤ EVDD ≤ 5.5V Cb = 100 pF, Rb = 3 kΩ		355		1420	ns
		2.0V ≤ EVDD ≤ 2.7V Cb = 100 pF, Rb = 5 kΩ		405		2070	ns

Note:

1. The value must also be equal to or less than fMCK/4.
2. Set the fMCK value to keep the hold time of SCLr = “L” and SCLr = “H”.

6.7.2 Serial interface IICA

(1) **I2C standard mode**

（T_A=–40～+105℃, 2.0V≤EVDD=VDD≤5.5V, V_{SS}=EVSS=0V）

Parameter	Symbol	Conditions	Spec		Unit
			MIN	MAX	
SCLA0 clock frequency	fSCL	Standard mode: f_{CLK}≥1MHz		100	kHz
Setup time of restart condition	$t_{SU:STA}$		4.7		μS
Hold time Note 1	$t_{HD:STA}$		4.0		μS
Hold time when SCLA0 = “L”	t_{LOW}		4.7		μS
Hold time when SCLA0 = “H”	t_{HIGH}		4.0		μS
Data setup time (reception)	$t_{SU:DAT}$		250		ns
Data hold time (transmission) Note 2	$t_{HD:DAT}$		0	3.45	μS
Setup time of stop condition	$t_{SU:STO}$		4.0		μS
Bus-free time	t_{BUF}		4.7		μS

Note:

1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark:

The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: Cb=400pF, Rb=2.7kΩ

(2) **I2C fast mode**

（T_A=–40～+105℃, 2.0V≤EVDD=VDD≤5.5V, V_{SS}=EVSS=0V）

Parameter	Symbol	Conditions	Spec		Unit
			MIN	MAX	
SCLA0 clock frequency	fSCL	Fast mode: f_{CLK}≥3.5MHz		400	kHz
Setup time of restart condition	$t_{SU:STA}$		0.6		μS
Hold time Note 1	$t_{HD:STA}$		0.6		μS
Hold time when SCLA0 = “L”	t_{LOW}		1.3		μS
Hold time when SCLA0 = “H”	t_{HIGH}		0.6		μS
Data setup time (reception)	$t_{SU:DAT}$		100		ns
Data hold time (transmission) Note 2	$t_{HD:DAT}$		0	0.9	μS
Setup time of stop condition	$t_{SU:STO}$		0.6		μS
Bus-free time	t_{BUF}		1.3		μS

Note:

1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Note: The maximum. value of C_b (communication line capacitance) and R_b (communication line pull-up resistance value) for each mode are as follows:

Fast mode: C_b=320pF, R_b=1.1kΩ

(3) **I2C fast mode plus**

（T_A=–40～+105℃, 2.0V≤EVDD=VDD≤5.5V, V_{SS}=EVSS=0V）

Parameter	Symbol	Conditions	Spec		Unit
			MIN	MAX	
SCLA0 clock frequency	fSCL	Fast mode plus: fCLK≥10MHz		1000	kHz
Setup time of restart condition	$t_{SU:STA}$		0.26		μS
Hold time Note 1	$t_{HD:STA}$		0.26		μS
Hold time when SCLA0 = “L”	t_{LOW}		0.5		μS
Hold time when SCLA0 = “H”	t_{HIGH}		0.26		μS
Data setup time (reception)	$t_{SU:DAT}$		50		ns
Data hold time (transmission) Note 2	$t_{HD:DAT}$		0	0.45	μS
Setup time of stop condition	$t_{SU:STO}$		0.26		μS
Bus-free time	t_{BUF}		0.5		μS

Note:

1. The first clock pulse is generated after this period when the start/restart condition is detected.
2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Note: The maximum. value of C_b (communication line capacitance) and R_b (communication line pull-up resistance value) for each mode are as follows:

Enhanced fast mode: C_b=120pF, R_b=1.1kΩ.

6.8 Analog Characteristics

6.8.1 A/D converter characteristics

Classification of A/D converter characteristics

Reference Voltage / Input channel	Reference voltage(+)=AV_{REFP} Reference voltage(–)=AV_{REFM}	Reference voltage(+)=V_{DD} Reference voltage(–)=V_{SS}
ANI0 ~ ANI15	Refer to 6.8.1(1)	Refer to 6.8.1(2)
Internal reference voltage Temperature sensor output voltage		

(1) When reference voltage(+)=AVREFP/ANI0, reference voltage (–)=AVREFM/ANI1

(TA=-40～+105℃, 2.0V≤AVREFP≤EVDD=VDD≤5.5V, VSS=0V, reference voltage(+)=AVREFP, reference voltage(–)=AVREFM=0V)

Parameter	Symb	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				12		bit
External input resistance	R_{AIN}	$R_{AIN} < (Ts / (fad \times Cadc \times \ln(2^{12+2})) - R_{ADC})$			10 note4		kΩ
Sampling switch resistance	R_{ADC}					1.5	kΩ
Sample holding capacitance	C_{ADC}				2		pF
Overall error note1	AINL	12-bit resolution	2.0V ≤AV_{REFP} ≤5.5V		3		LSB
Conversion time note3	t_{CONV}	12-bit resolution Target pin:ANI2 ~ ANI15	2.0V≤VDD≤5.5V	45			Tmclk
		12-bit resolution Target pin:Internal reference voltage,and temperature sensor output voltage, PGAoutput voltage	2.0V≤VDD≤5.5V	72			Tmclk
Zero-scale error Note 1	E_{ZS}	12-bit resolution	2.0V ≤AV_{REFP} ≤5.5V		0		LSB
Full-scale error Note 1	E_{FS}	12-bit resolution	2.0V ≤AV_{REFP} ≤5.5V		0		LSB
Integral linearity error Note 1	ILE	12-bit resolution	2.0V ≤AV_{REFP} ≤5.5V	-1		1	LSB
Differential linearity error Note 1	DLE	12-bit resolution	2.0V ≤AV_{REFP} ≤5.5V	-1.5		1.5	LSB
Analog input voltage	V_{AIN}	ANI2 ~ ANI15		0		AV_{REFP}	V
		Internal reference voltage (2.0V≤VDD≤5.5V)		V_{BGR} note2			V
		Temperature sensor output voltage (2.0V≤VDD≤5.5V)		V_{TMPS25} note2			V

Note 1. Excludes quantization error (±1/2 LSB).

2. Refer to "6.8.2 Temperature sensor characteristics/internal reference voltage characteristic".

3. Tmclk is the operating clock cycle of AD, and the maximum operating frequency is 48MHz.

4. It is guaranteed by the design and not tested in mass production. The typical value is the calculated value under the condition of default sampling period Ts=13.5 and conversion speed fad=48 MHz.

(2) When reference voltage (+)=VDD, reference voltage (–)=VSS

（TA=–40～ +105℃, 2.0V≤ EVDD= VDD≤ 5.5V, VSS=EVSS=0V, reference voltage (+)=VDD, reference voltage (–)=VSS）

Parameter	Symb	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				12		bit
External input resistance	R_{AIN}	$R_{AIN} < (Ts / (fad \times Cadc \times \ln(2^{12+2})) - R_{ADC})$			10note4		
Sampling switch resistance	R_{ADC}					1.5	
Sample holding capacitance	C_{ADC}				2		
Overall error note1	AINL	12-bit resolution	2.0V ≤AV_{REFP} ≤5.5V		6		LSB
Conversion time note3	t_{CONV}	12-bit resolution Target pin:ANI0 ~ ANI15	2.0V≤VDD≤5.5V	45			Tmclk
		12-bit resolution Target pin:Internal reference voltage,and temperature sensor output voltage, PGAoutput voltage	2.0V≤VDD≤5.5V	72			Tmclk
Zero-scale error Note 1	E_{ZS}	12-bit resolution	2.0V ≤AV_{REFP} ≤5.5V		0		LSB
Full-scale error Note 1	E_{FS}	12-bit resolution	2.0V ≤AV_{REFP} ≤5.5V		0		LSB
Integral linearity error Note 1	ILE	12-bit resolution	2.0V ≤AV_{REFP} ≤5.5V	-2		2	LSB
Differential linearity error Note 1	DLE	12-bit resolution	2.0V ≤AV_{REFP} ≤5.5V	-3		3	LSB
Analog input voltage	V_{AIN}	ANI0 ~ ANI7		0		V_{DD}	V
		ANI8 ~ ANI15		0		EV_{DD}	V
		Internal reference voltage （2.0V≤VDD≤5.5V）		V_{BGR} note2			V
		Temperature sensor output voltage （2.0V≤VDD≤5.5V）		V_{TMPS25} note2			V

Note 1. Excludes quantization error (±1/2 LSB).

2. Refer to "6.8.2 Temperature sensor characteristics/internal reference voltage characteristic".

3. Tmclk is the operating clock cycle of AD, and the maximum operating frequency is 48MHz.

4. It is guaranteed by the design and not tested in mass production. The typical value is the calculated value under the condition of default sampling period Ts=13.5 and conversion speed fad=48MHz.

6.8.2 Temperature sensor characteristics/internal reference voltage characteristic

（TA=–40～+105℃, 2.0V≤VDD≤5.5V, VSS=EVSS=0V）

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Temperature sensor output voltage	VTMPS25	TA=25℃		1.09		V
Internal reference voltage Temperature coefficient	VBGR	TA=–40～10℃	1.25note1	1.45	1.65 note1	V
		TA=10～70℃	1.38	1.45	1.5	V
		TA=70～105℃	1.32	1.45	1.55	V
Operation stabilization wait time	FVTMPS			-3.5		mV/℃
Temperature sensor output voltage	tAMP		5			μs

Note 1. The low temperature specification value is guaranteed by the design, and the low temperature condition is not measured for mass production.

6.8.3 D/A converter characteristics

（TA=–40～+105℃, 2.0V≤EVDD=VDD≤5.5V, VSS=EVSS=0V）

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Resolution	RES					8	bit
Overall error	AINL	Rload=4MΩ	2.0V≤VDD≤5.5V	-2.5		2.5	LSB
Settling time	tSET	Cload=20pF	2.7V ≤ VDD ≤ 5.5V			3	μs
			2.0V ≤ VDD ＜ 2.7V			6	μs
Output impedance	RO	Rload=4MΩ	2.0V≤VDD≤5.5V	4.7		8	kΩ

6.8.4 Comparator

（T_A=–40～+105℃, 2.0V≤EVDD=VDD≤5.5V, V_{SS}=EV_{SS}=0V）

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Input offset voltage	V_{OFFSET}				±10	±40	mV
Input voltage range	V_{IN}			0		VDD	V
Internal reference voltage deviation	ΔV_{IREF}	CmRVM register value : 7FH ~ 80H (m = 0, 1)				±2	LSB
		Other than above				±1	LSB
Response Time	tCR,tCF	Input amplitude±100mV			70	150	ns
Operation stabilization Time Note 1	T_{STB}	CMPn=0->1	VDD= 3.3 ~ 5.5V			1	μs
			VDD= 2.0 ~ 3.3V			3	
Reference voltage stabilization wait time	tVR	CVRE=0->1 Note2				20	μs
Operation current	I_{CMPDD}	Separately, it is defined as the operation current of peripheral functions.					

Note1:Time taken until the comparator satisfies the DC/AC characteristics after the comparator operation enable signal is switched (CMPnEN = 0 → 1).

Note2:Enable comparator output (CnOE bit = 1; n = 0 to 1) after enabling operation of the internal reference voltage generator (by setting the CVREm bit to 1; m = 0 to 1) and waiting for the operation stabilization time to elapse.

6.8.5 PGA

（T_A=–40～+105℃, 2.0V≤EVDD=VDD≤5.5V, V_{SS}=EV_{SS}=0V）

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Input offset voltage	V_{OS}				±3	±10	mV
Input voltage range	V_I			0		0.9xVDD/ Gain	V
Output voltage range	V_{OH}			0.93xVDD			V
	V_{OL}					0.07xVDD	V
Gain error		x4		-1		1	%
		x8		-1		1	%
		x10		-1		1	%
		x12		-2		2	%
		x14		-2		2	%
		x16		-2		2	%
		x32		-3		3	%
Slew rate	SR_R	Rising Vin= 0.1VDD/gain to 0.9VDD/gain. 10 to 90% of output voltage amplitude	4.0 V ≤ VDD ≤ 5.5 V (Other than x32)	3.5			V/us
			4.0 V ≤ VDD ≤ 5.5 V (x32)	3.0			
			2.0 V ≤ VDD ≤ 4.0V	0.5			
	SR_F	Falling Vin= 0.1VDD/gain to 0.9VDD/gain. 90 to 10% of output voltage amplitude	4.0 V ≤ VDD ≤ 5.5 V (Other than x32)	3.5			
			4.0 V ≤ VDD ≤ 5.5 V (x32)	3.0			
			2.0 V ≤ VDD ≤ 4.0V	0.5			
Reference voltage stabilization wait time Note 1	t_{STB}	x4				5	uS
		x8				5	uS
		x10				5	uS
		x12				10	uS
		x14				10	uS
		x16				10	uS
		x32				10	uS
Operation current	IPGA	Separately, it is defined as the operation current of peripheral functions.					

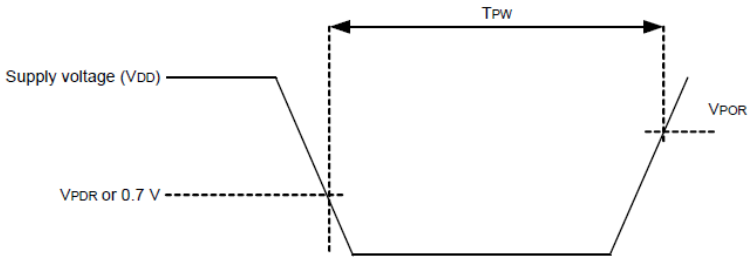
Note1.Time required until a state is entered where the DC and AC specifications of the PGA are satisfied after the PGA operation has been enabled (PGAEN = 1).

6.8.6 POR circuit characteristics

（T_A=–40～+105℃, V_{SS}=0V）

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Power on/down reset threshold	V_{POR}	Voltage threshold on VDD rising		1.50	2.0	V
	V_{PDR}	Voltage threshold on VDD falling	1.37	1.45		V
Minimum pulse width (Note 1)	T_{PW}		300			μs

Note1. Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}. This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



6.8.7 LVD circuit characteristics

1, **Reset Mode and Interrupt Mode**

（T_A=–40～+105℃, $V_{PDR} \le V_{DD} \le 5.5V$, V_{SS}=0V）

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Voltage detection threshold	VLVD0	Rising edge		4.06	4.26	V
		Falling edge	3.78	3.98		V
	VLVD1	Rising edge		3.75		V
		Falling edge		3.67		V
	VLVD2	Rising edge		3.13		V
		Falling edge		3.06		V
	VLVD3	Rising edge		3.02		V
		Falling edge		2.96		V
	VLVD4	Rising edge		2.92		V
		Falling edge		2.86		V
	VLVD5	Rising edge		2.81		V
		Falling edge		2.75		V
	VLVD6	Rising edge		2.71		V
		Falling edge		2.65		V
	VLVD7	Rising edge		2.61		V
		Falling edge		2.55		V
	VLVD8	Rising edge		2.50		V
		Falling edge		2.45		V
	VLVD9	Rising edge		2.09	2.16	V
		Falling edge	1.97	2.04		V
Minimum pulse width	tLW		300			μs
Detection delay time					300	μs

2, **Interrupt Mode & Reset Mode**

（T_A=–40～+105℃, V_{PDR} ≤V_{DD}≤5.5V, V_{SS}=0V）

Parameter	Symbol	Conditions			MIN	TYP	MAX	Unit
Interrupt Mode & Reset Mode	V_{LVDB0}	V_{POC2}、V_{POC1}、V_{POC0}=0、0、1，falling reset voltage			1.78	1.84		V
	V_{LVDB1}	LVIS1、LVIS0=1、0		Rising release reset		1.98	2.04	V
				Falling interrupt voltage	1.88	1.94		V
	V_{LVDB2}	LVIS1、LVIS0=0、1		Rising release reset		2.09		V
				Falling interrupt voltage		2.04		V
	V_{LVDB3}	LVIS1、LVIS0=0、0		Rising release reset		3.13		V
				Falling interrupt voltage		3.06		V
	V_{LVDC0}	V_{POC2}、V_{POC1}、V_{POC0}=0、1、0，falling reset voltage				2.45		V
	V_{LVDC1}	LVIS1、LVIS0=1、0		Rising release reset		2.61		V
				Falling interrupt voltage		2.55		V
	V_{LVDC2}	LVIS1、LVIS0=0、1		Rising release reset		2.71		V
				Falling interrupt voltage		2.65		V
	V_{LVDC3}	LVIS1、LVIS0=0、0		Rising release reset		3.75		V
				Falling interrupt voltage		3.67		V
	V_{LVDD0}	V_{POC2}、V_{POC1}、V_{POC0}=0、1、1，falling reset voltage				2.75		V
	V_{LVDD1}	LVIS1、LVIS0=1、0		Rising release reset		2.92		V
				Falling interrupt voltage		2.86		V
	V_{LVDD2}	LVIS1、LVIS0=0、1		Rising release reset		3.02		V
				Falling interrupt voltage		2.96		V
	V_{LVDD3}	LVIS1、LVIS0=0、0		Rising release reset		4.06	4.26	V
				Falling interrupt voltage	3.78	3.98		V

6.8.8 Power supply voltage rising slope characteristics

（T_A=-40～+105℃, V_{SS}=0V）

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Reset time	T_{RESET}			1		ms
Power supply voltage rising slope	SVDD				54	V/ms

6.9 Memory characteristics

6.9.1 Flash Memory

（T_A=–40～+105℃, 2.0V≤EVDD=VDD≤5.5V, V_{SS}=EV_{SS}=0V）

Symbol	Parameter	Conditions	MIN	MAX	Unit
Tprog	Word Program(32bit)	Ta=–40～+105℃	24	30	μs
Terase	Sector erase(512B)	Ta=–40～+105℃	4	5	ms
	Chip erase	Ta=–40～+105℃	20	40	ms
N_{END}	Endurance	Ta=–40～+105℃	100		kcycle
t_{RET}	Data retention	100 kcycle(2) at Ta = 105℃	20		Years

Note1:Data based on characterization results, not tested in production.

Note2:Cycling performed over the whole temperature range.

6.9.2 RAM Memory

（T_A=–40～+105℃, 2.0V≤EVDD=VDD≤5.5V, V_{SS}=EV_{SS}=0V）

Symbol	Parameter	Conditions	MIN	MAX	Unit
Vramhold	RAM Hold Voltage	Ta=–40～+105℃	0.8		V

Remark: It is guaranteed by the design and not tested in mass production.

6.10 Electrical sensitivity characteristics

6.10.1 Electrostatic discharge (ESD)

Symbol	Parameter	Conditions	Class
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25°C, JESD22-A114	3A

Note: Data based on characterization results, not tested in production.

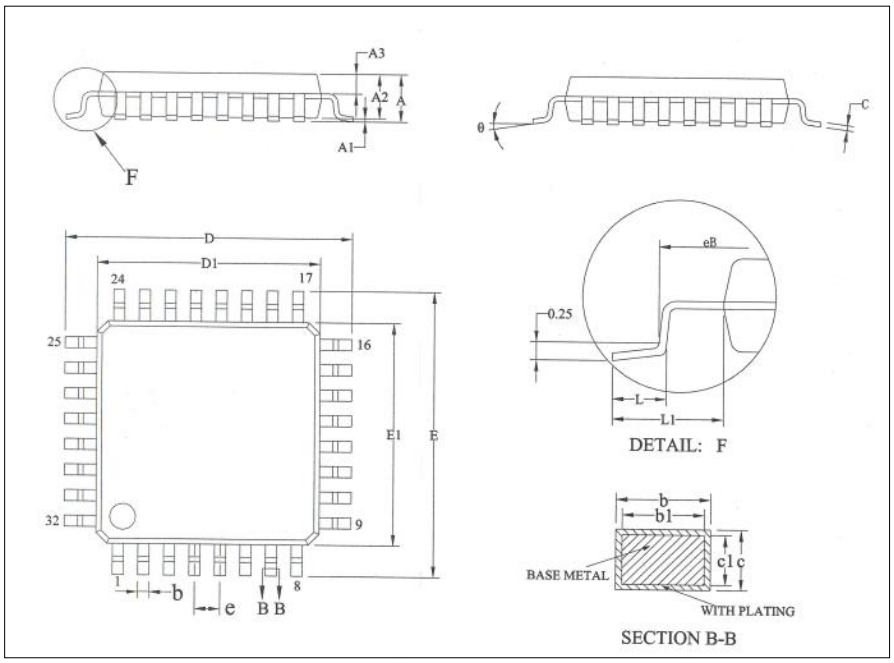
6.10.2 Static latch-up(LU)

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +25°C, JESD78F	I levelA

Note: Data based on characterization results, not tested in production.

7 Package Drawings

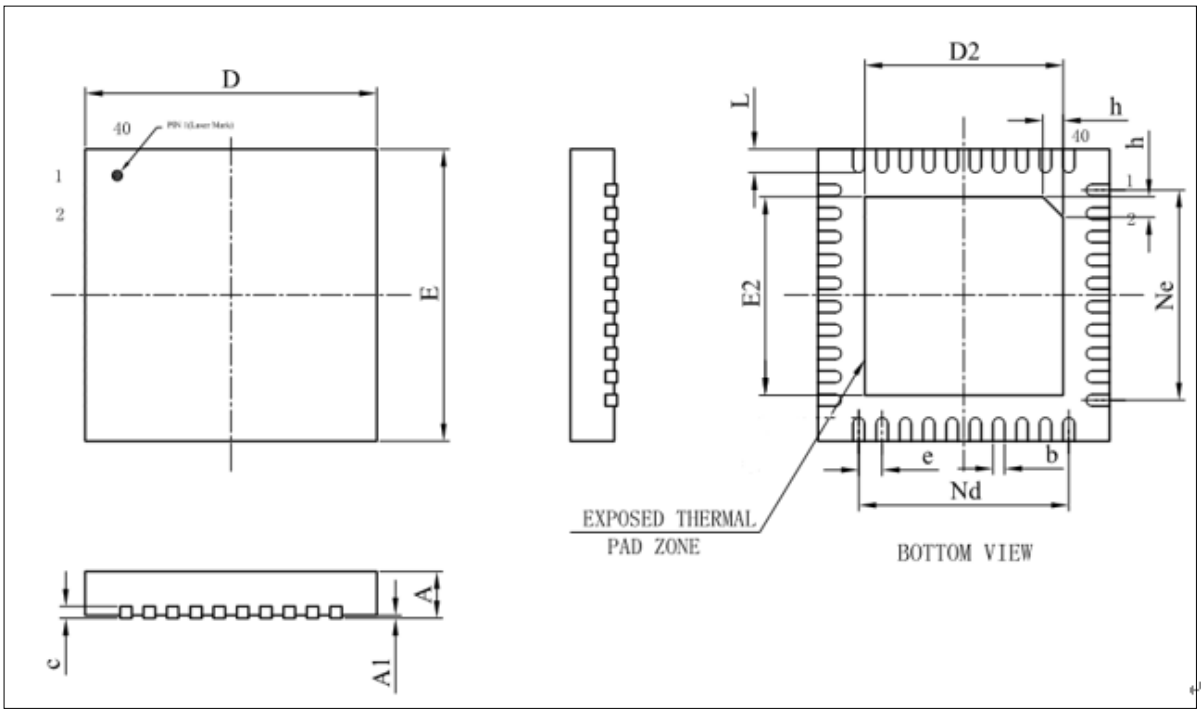
7.1 LQFP32 (7x7mm, 0.8mm)



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	-	0.41
b1	0.32	0.35	0.38
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.80BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0°	-	7°

Caution: Package dimensions do not include mold flash or gate burrs.

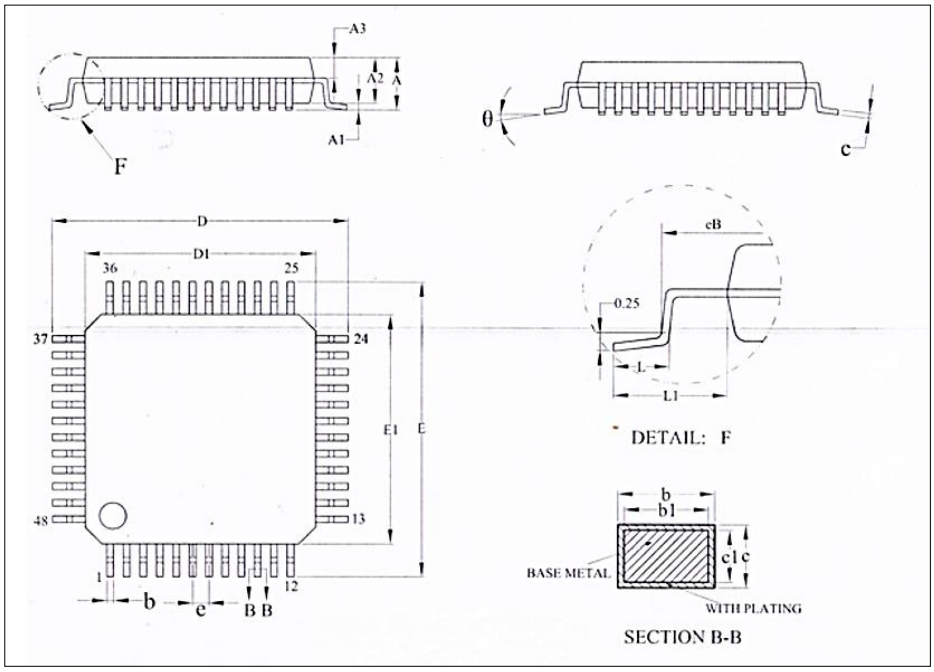
7.2 QFN40 (5x5mm, 0.4mm)



Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.30	-	3.80
e	0.40BSC		
Ne	3.60BSC		
Nd	3.60BSC		
E	4.90	5.00	5.10
E2	3.30	-	3.80
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Caution: Package dimensions do not include mold flash or gate burrs.

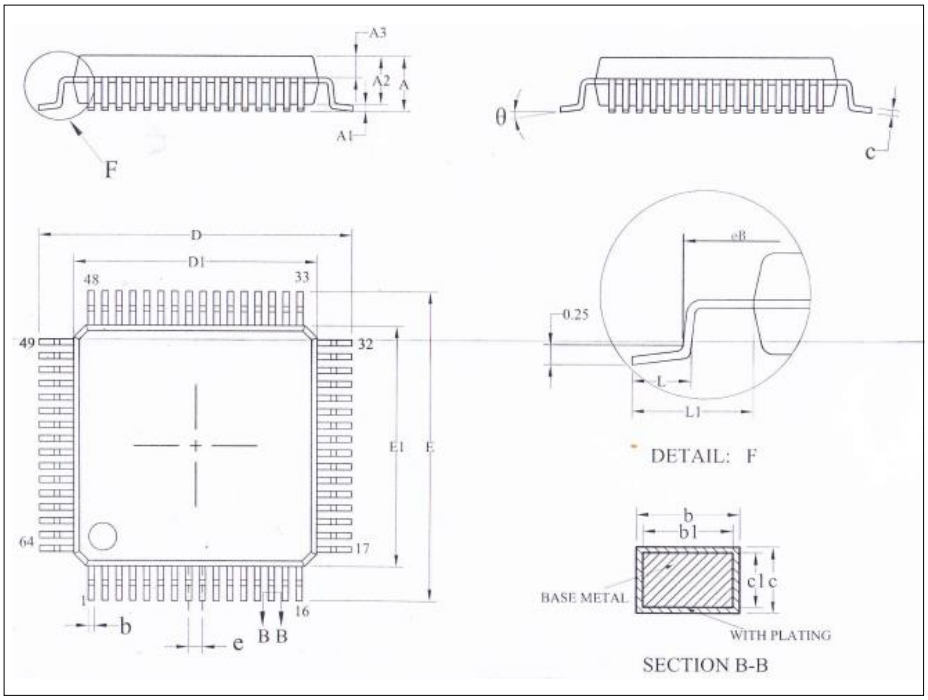
7.3 LQFP48 (7x7mm, 0.5mm)



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.30	1.40	1.50
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.50BSC		
L	0.43	-	0.75
L1	1.00REF		
θ	0°	-	8°

Caution: Package dimensions do not include mold flash or gate burrs.

7.4 LQFP64 (7x7mm, 0.4mm)



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.16	-	0.24
b1	0.15	0.18	0.21
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.40BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0°	-	7°

Caution: Package dimensions do not include mold flash or gate burrs.

8 Revision History

Rev.	date	Description	
		Page/Chapter	Changes
2.0	2019.09.09	—	Original Issue
	2019.11.01	1.2, 6.4.2	Product list and IDD result Update.
2.1	2020.01.07	Features, 1.2, 5.22	The ADC conversion rate is updated, the product model is added (BAT32G137GH48FA), and the header is updated.
2.2	2020.04.11	1.2, 4, 6.1	The 64K model was cancelled and the 128K GH series was replaced, adding the CAN bus function. A schematic diagram of a typical application peripheral circuit is added.
2.3	2020.04.20	6.3, 6.5.1	VOHL spec update（stronger）.
2.4	2020.06.15	6.9, 6.10	Added Memory and Electrical sensitivity feature description chapters.
2.5	2020.07.07	6.1	The schematic diagram of a typical application peripheral circuit is updated. Modify some punctuation and fonts.
2.5.1	2022.11.16	6.10	Optimize EMS features
	2023.02.13	1.2 1.3.2 4.1 4.3 5.1 5.22 6 6.4.2,6.8.2	Add product selection table Correct the pin diagram Correct the product pin function description Schematic diagram of adding port type Optimization description CAN controller content supplement Electrical property data update Add a note on low temperature conditions.
2.5.2	2023.08.28	1.1	Modified 1.1 Introduction
2.5.3	2023.01.15	5.1,3.2	Corrected the content description of multiple PWM Modify the XT1 clock oscillation starting capacitance value Update cover information
2.5.4	2024.01.25	6.3	Add input current parameters
2.5.5	2024.03.20	6.1	Modified Typical application peripheral circuit
2.5.6	2024.07.17	7.2, 7.3 6.8.1,6.8.8	Modified package dimensions Update parameter value
2.5.7	2024.09.05	6.10.2	Modify Latch_up test criteria
	2024.09.20	Cover page	Revised the cover page
	2024.10.24	4.1.1 -	Correct the 32pin port functional description Delete incorrect content in the function description
2.5.8	2025.01.20	6.4.1	Add X1 clock oscillator transconductance (gm) parameter
2.5.9	2025.06.03	5.25	Delete section 5.25with errors